Preliminary publication of JEDEC Semiconductor Memory Ballot

This Ballot was developed by JEDEC Committee JC-45 and approved by the JEDEC Board of Directors. It is published here in preliminary form, prior to being integrated into JEDEC Standard JESD21C and published in final form.

Title of Ballot: DDR4 UDIMM Design Specification Annex D

Council Ballot Number: JCB-14-002

Committee Ballot Number: 45.3-13-455

Committee Item Number: 2231.09

Date of Council Approval: Feb 2014

Background: This proposal was balloted as JC-45.3-13-455 on November 12, 2013 and expired on December 4, 2013. The voting results were reported at the December, 2014 JC-45 Committee meeting at which time the ballot was approved for Board of Directors submittal.

Annex D - Raw Card D

DDR4 Unbuffered DIMM Design File

Raw Card	Applicable Design File	Applicable BOM
D0	PC4-UDIMM_V080_RC_D0_20131028.brd	PC4-UDIMM_V080_RC_D0__20131028_BOM.xlsx
Note: "Reference" design file updates will be released as needed. This DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only. In these cases the design files will not be updated.		

Module Configuration

DIMM		SDRAM		# of SDRAM die Min/Max	# of Logical Ranks per DIMM Min/Max	# of Package Ranks per DIMM Min/Max	# of Address bits row/col	MO-309 variation
Maximum Capacity	Organization	Die Density	Organization					
2GB	256Mx72	2Gbit	256M x 8	9/9	1	1	14/10[1]	AAxA
4GB	512Mx72	4Gbit	512G x 8	9/9	1	1	15/10[1]	AAxA
8GB	1Gx72	8Gbit	1G x 8	9/9	1	1	16/10	AAxA
16GB	2Gx72	16Gbit	2G x 8	9/9	1	1	17/10	AAxA
1. Address A16 is the highest address bit used based on it being multiplexed with RAS_n								

SDRAM Configuration

Supported DRAM Outline (Width x Length) max.	# of Banks in SDRAM BA/BG	SDRAM Package Type	Package Type	MO-207 variation
11.0 x 13.0	2/2	78 Ball FBGA	SDP	DW-z
Note: SDP is a Single Die per Package.				

Supported Speeds

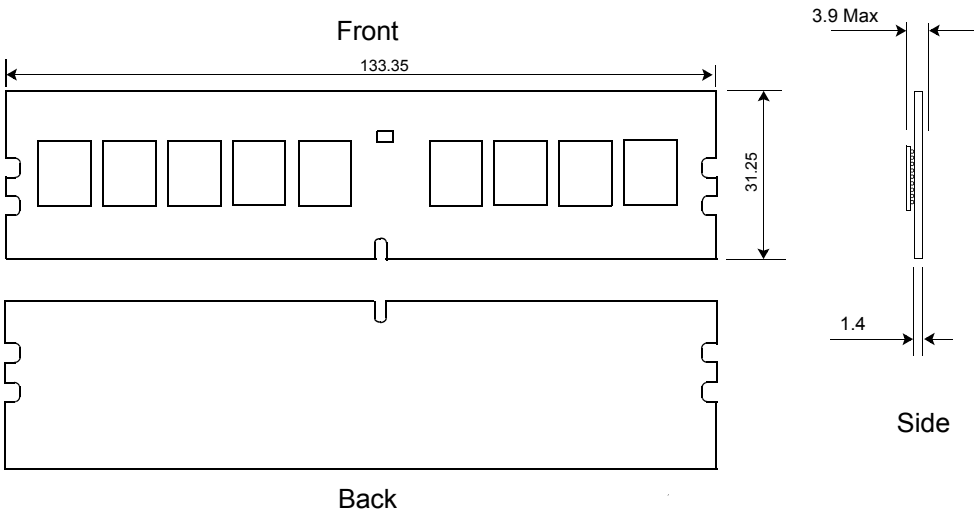
Raw Card	Speed	PC4-1333	PC4-1600	PC4-1866	PC4-2133	PC4-2400	PC4-2666	PC4-3200	Notes
D0	DDR4	P	P	P	P				1, 2
Note 1: X reflects speed grades approved from previous ballots. Note 2: P denotes speed grades being proposed for this most recent ballot									

Design Deviations

1. None.

Proposed

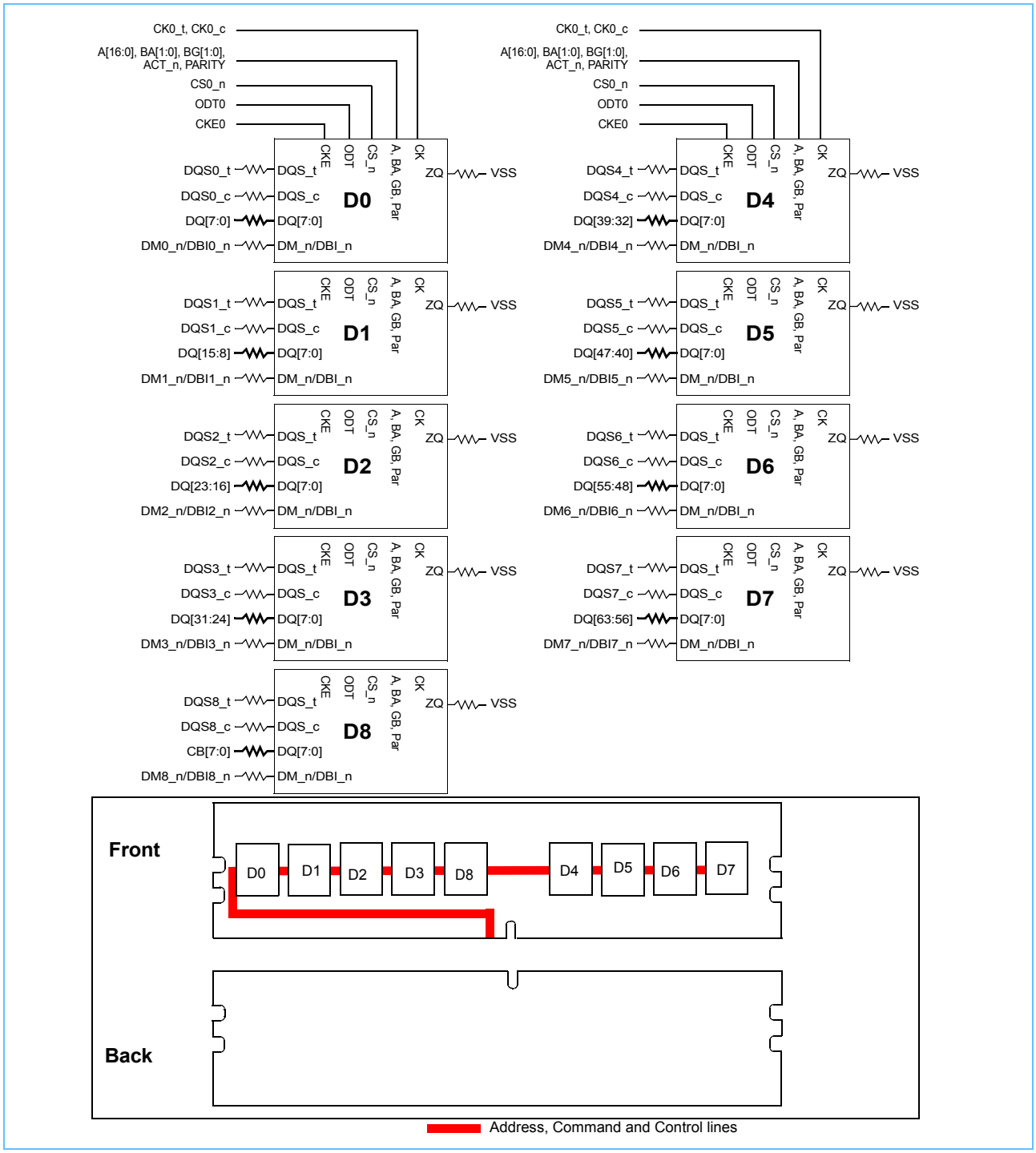
General Layout



Note 1: Refer to MO-309 for more detailed information.
Note 2: Variation is AAxA (**A** Module height, **A** Moduile thickness, **x** plating, **A** Key Position).
Note 3: Module thickness may vary with DRAM thickness and passive components.

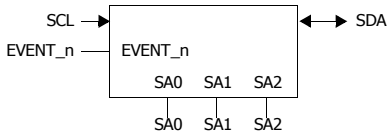
Functional Block Diagram

x72 DIMM, populated as one package rank of x8 DDR4 SDRAMs (Part 1 of 1)

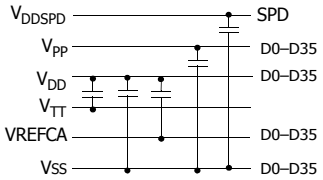


Proposed

Note 1: CK1_t, CK1_c terminated with 120Ω ± 5% resistor.
Note 2: Unless otherwise noted resistors are 15Ω ± 5%.
Note 3: ZQ resistors are 240Ω ± 1%. For all other resistor values refer to the appropriate wiring diagram.



Sensor PD with Thermal Sensor



Input Loading and Test Points

Input Loading

Signal Names	Input to Device	Loads
CK0_t, CK0_c	SDRAMs	9
CK1_t, CK1_c[2]	Termination Resistor Only	1[1]
RESET_n	SDRAMs	9
CKE0, ODT0	SDRAMs	9
Ax, BAx, BGx, RAS_n, CAS_n, WE_n, PARITY, ACT_n	SDRAMs	9
CS0_n	SDRAMs	9
DQ, CB, DQS_t, DQS_c	SDRAM	1
DMx_n/DBIx_n	SDRAM	1
SCL,SDA,SA[2:0],EVENT_n	SPD	1
ALERT_n	SDRAM	9
Note 1: Connected but not used.		

Test Point Locations

Signal Group	Signal	Signal locations
Address/Command/ Control/PARITY	ALL	Termination resisitors on the end of the module
DQ,CB,DM_n,DBI_n	ALL	15 Ohm resistors
DQS_t, DQS_c	ALL	15 Ohm resistors
Clock	ALL	Termination resistors.
Note 1: Refer to the registration package for additional test point information.		

Proposed

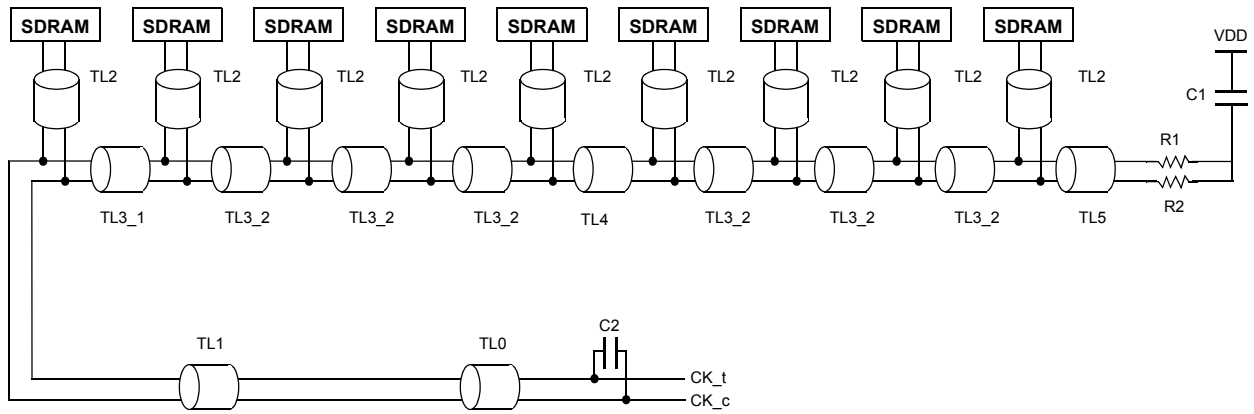
DQ Map for CRC

See Common section of the DDR4 UDIMM Design Specification for information on interpreting the DQ Mapping table.

SPD Values for DQ Mapping

DQ Bits as defined by connector	SPD Byte (Decimal)	SPD Value (Hex)	DQ Bits as defined by connector	SPD Byte (Decimal)	SPD Value (Hex)
DQ0, DQ1, DQ2, DQ3	60	16	DQ32, DQ33, DQ34, DQ35	70	16
DQ4, DQ5, DQ6, DQ7	61	36	DQ36, DQ37, DQ38, DQ39	71	36
DQ8, DQ9, DQ10, DQ11	62	16	DQ40, DQ41, DQ42, DQ43	72	16
DQ12, DQ13, DQ14, DQ15	63	36	DQ44, DQ45, DQ46, DQ47	73	36
DQ16, DQ17, DQ18, DQ19	64	16	DQ48, DQ49, DQ50, DQ51	74	16
DQ20, DQ21, DQ22, DQ23	65	36	DQ52, DQ53, DQ54, DQ55	75	36
DQ24, DQ25, DQ26, DQ27	66	16	DQ56, DQ57, DQ58, DQ59	76	16
DQ28, DQ29, DQ30, DQ31	67	36	DQ60, DQ61, DQ62, DQ63	77	36
CB0, CB1, CB2, CB3	68	16			
CB4, CB5, CB6, CB7	69	36			

Clock Input Net Structure



Trace Lengths for Clock to SDRAM load Net Structures

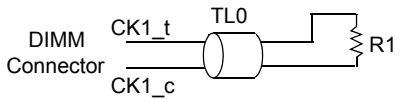
Signal	TL0 (MS)	TL1	TL2 (MS)	Length to First SDRAM TL0+TL1+TL2 with Via Compensation Equivalent SL	TL3_1 (SL)	TL3_2 (SL)	TL4 (SL)	TL5 (MS+SL)	R1,R2 (Ohms)	C1 (uF)	C2 (uF)	Notes
CK0_t	4.12	107.8	0.57	115.58	20	14.73	19.73	12.56	39 ± 5%	0.01	0	1,2
CK0_c	4.12	107.8	0.57	115.58	20	14.73	19.73	12.86				1,2

1. All distances are given in millimeters and must be kept within a tolerance of ±0.1 mm..
2. Any MS(Microstrip) sections are convertedto equivalent SL (Stripline) by dividing by 1.1. Any imbalance in vias is compensated as 2 times the Z axis length of the travelled path.

Proposed

Net Structure for Unused Clock

Net Structure Routing for Unused Clock DIMM Terminatio



Trace Lengths for Unused Clock DIMM Termination Net Structures

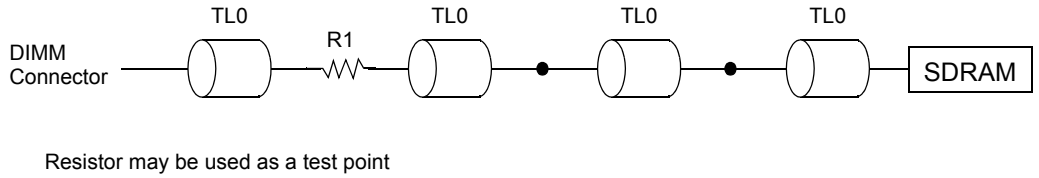
Signal	TL0	R1 (Ohms)	Notes
CK1_t	4.07	120 ± 5%	1
CK1_c	4.08		1

1. All distances are given in millimeters and must be kept within a tolerance of ±0.8 millimeter.

Proposed

Net Structure for DQ, DQS_t, DQS_c, CB, DM_n/DBI_n

Data Net Structure - DQ, CB, DQS_t, DQS_c



Resistor may be used as a test point

This group includes DQ[63:0], CB[7:0], DQS[17:0]_t, DQS[17:0]_c.

Recommend delays for all nets, as described in the following tables.

Trace Lengths for DQ[63:0], CB[7:0], DQS[8:0]_t, DQS[8:0]_c,DM[8:0]_n,DBI[8:0]_n

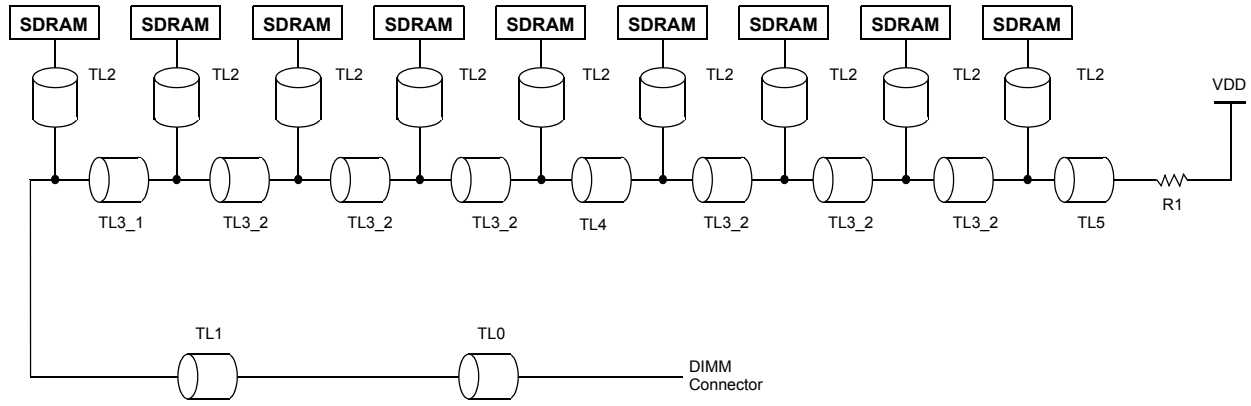
DQ signals	TL0		TL1		TL2		TL3		Compen-sated Length TL0 + TL1 + TL2 + TL3	R1 (Ohms)	Notes
	Min	Max	Min	Max	Min	Max	Min	Max			
DQ[7:0], DQS0_t, DQS0_c	3.03	3.35	0.95	1.62	10.00	13.86	0.57	1.85	18.71	15 ± 5%	1,2
DQ[15:8], DQS1_t, DQS1_c	3.03	3.35	0.95	1.62	12.47	16.32	0.57	1.85	21.17	15 ± 5%	1,2
DQ[23:16], DQS2_t, DQS2_c	3.03	3.35	0.95	1.62	15.81	19.66	0.57	1.85	24.51	15 ± 5%	1,2
DQ[31:24], DQS3_t, DQS3_c	3.13	3.56	0.95	1.62	18.82	22.72	0.57	1.85	27.66	15 ± 5%	1,2
CB[7:0], DQS8_t, DQS8_c	3.28	3.60	0.95	1.62	23.23	26.75	0.57	1.85	31.82	15 ± 5%	1,2
DQ[39:32], DQS4_t, DQS4_c	3.28	3.60	0.95	1.62	14.17	18.03	0.57	1.85	23.11	15 ± 5%	1,2
DQ[47:40], DQS5_t, DQS5_c	3.18	3.56	0.95	1.62	10.92	14.74	0.57	1.85	19.72	15 ± 5%	1,2
DQ[55:48], DQS6_t, DQS6_c	3.03	3.35	0.95	1.62	9.24	13.10	0.57	1.85	17.95	15 ± 5%	1,2
DQ[63:56], DQS7_t, DQS7_c	3.03	3.35	0.95	1.62	8.11	11.96	0.57	1.85	16.81	15 ± 5%	1,2

1. All distances are given in millimeters and must be kept within a tolerance of ±0.1 mm..
2. Any MS(Microstrip) sections are convertedto equivalent SL (Stripline) by dividing by 1.1. Any imbalance in vias is compensated as 2 times the Z axis length of the travelled path.

Proposed

Address and Command Net Structure Routing

A[16:0], BA[1:0], BG[1:0], PARITY, ACT_n



Trace Lengths Address and Command Net Structures

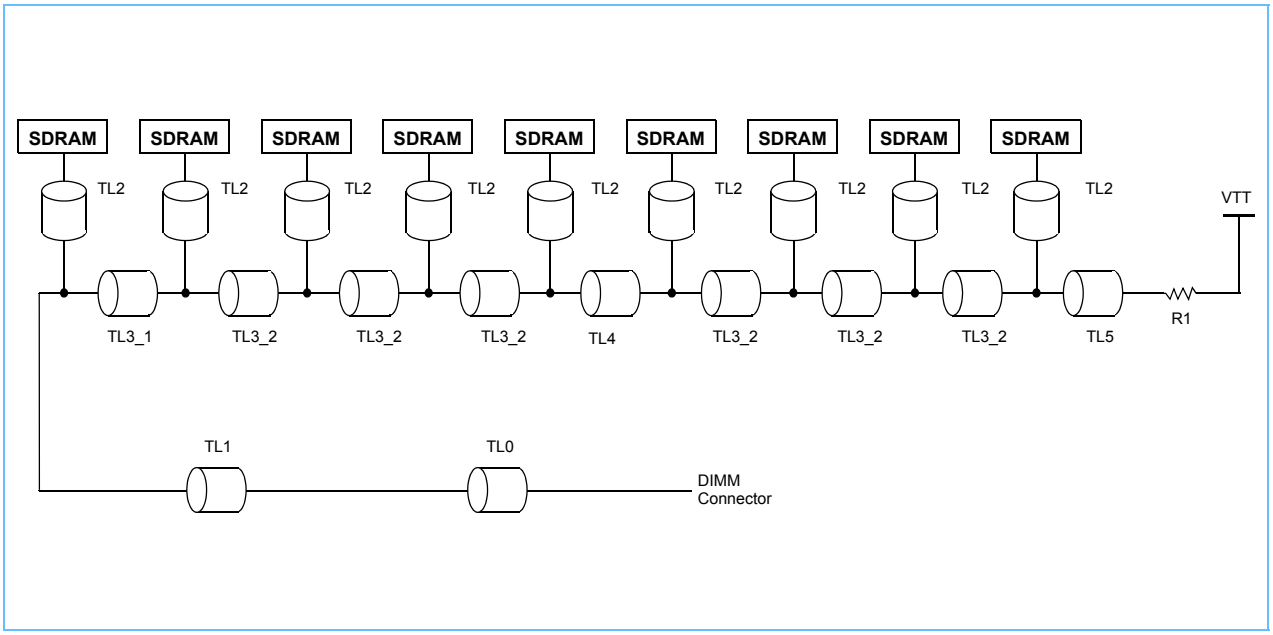
Signal	TL0 (MS)	TL1	TL2 (MS)	Length to First SDRAM TL0+TL1+TL2 with Via Compensation Equivalent SL	TL3_1 (SL)	TL3_2 (SL)	TL4 (SL)	Last SDRAM TL0+TL1+TL3's+TL4+ TL2+Via Compensation Equivalent SL	TL5 (MS+SL)	R1 (Ohms)	Notes
Min	3.54	91.25	0.57	115.4	19.9	14.6	19.6	243.6	5.96	39 ± 5%	1,2,3
Max	23.28	109.18	1.25	115.6	20.1	14.8	19.8	243.8	12.35		1,2,3

1. All distances are given in millimeters and must be kept within a tolerance of ±0.1 mm..
2. Any MS(Microstrip) sections are convertedto equivalent SL (Stripline) by dividing by 1.1. Any imbalance in vias is compensated as 2 times the Z axis length of the travelled path.
3. TL5 lengths are not required to be met.

Proposed

Post Register Control Net Structure Routing

CS[0]_n, CKE[0], ODT[0]



Trace Lengths of Control Net Structures

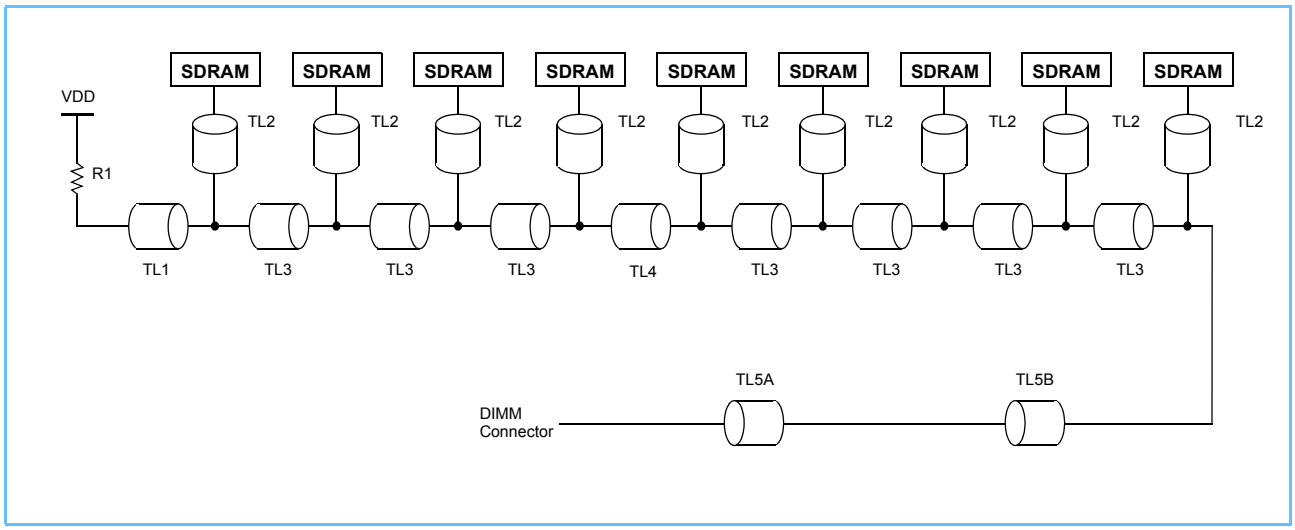
Signal	TL0 (MS)	TL1	TL2 (MS)	Length to First SDRAM TL0+TL1+TL2 with Via Compensation Equivalent SL	TL3_1 (SL)	TL3_2 (SL)	TL4 (SL)	Last SDRAM TL0+TL1+TL3's+TL4+ TL2+Via Compensation Equivalent SL	TL5 (MS+SL)	R1 (Ohms)	Notes
Min	5.05	105.44	1.00	115.56	19.9	14.6	19.6	243.6	8.44	39 ± 5%	1,2,3
Max	5.11	107.24	1.02	115.57	20.1	14.8	19.8	243.8	9.36		1,2,3

1. All distances are given in millimeters and must be kept within a tolerance of ±0.1 mm..
2. Any MS(Microstrip) sections are convertedto equivalent SL (Stripline) by dividing by 1.1. Any imbalance in vias is compensated as 2 times the Z axis length of the travelled path.
3. TL5 lengths are not required to be met.

Proposed

ALERT_n Net Structures

ALERT_n Net

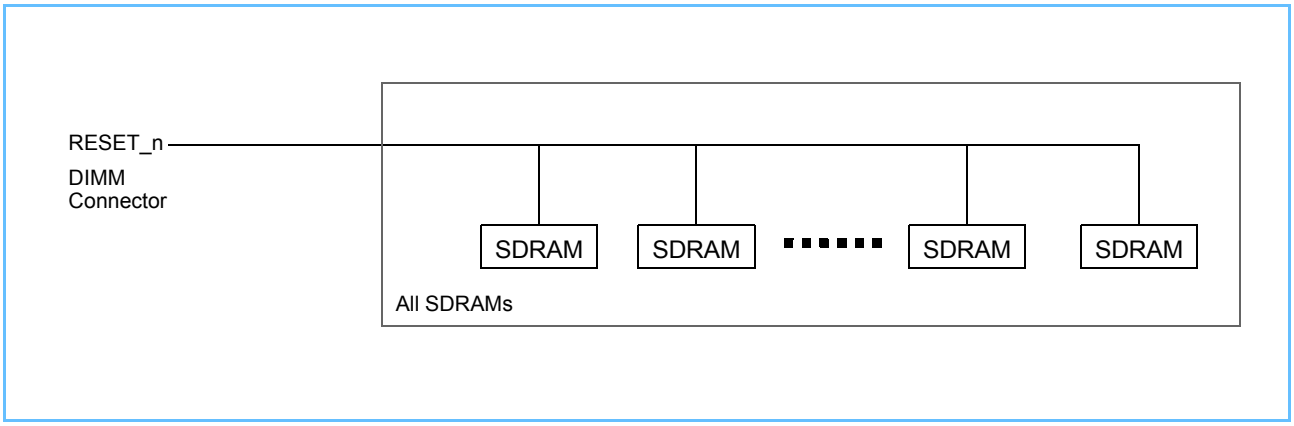


TL1	TL2	TL4	TL3_2	TL3_1	TL4	TL5	R1 (Ohms)	Notes
3.55	0.57	18.04	13.60	14.13	67.31	24.64	59 ± 5%	1
1. All distances are given in millimeters and must be kept within a tolerance of ± 1.0mm.								

Proposed

RESET_n Net Structures

RESET_n Net



RESET_n Net Total Length

Total Net Length		
RESET_n	215.55	1

1. Total length of all traces together (in millimeters) is specified and must be kept within a tolerance of ± 10%
2. RESET_n routing follows the address routing. Individual lengths are not specified.

Cross Section Recommendations

PCBs should contain solid ground plane and power plane layers as far as possible. Minimum trace width is 0.075 mm.

The PCB edge connector contacts shall be gold plated.

Any exceptions to these design rules has been identified in the front of this annex.

PCB Fabrication Table

Layer	Layer Description	Single-ended Impedances		Differential Impedances		Copper oz	Dielectric Thickness (um)
		Trace Width (mm)	Impedance (Ohms)	Trace Width/Spacing (mm / mm)	Impedance (Ohms)		
1	DQ	0.10	50 ±10%	0.10/0.10	83 ±15%	1/3 + Plating	
	Address/CK	0.075	55 ±10%	0.075/0.10	93 ±15%		
	Address/CK	0.15	40 ±10%	0.15/0.10	70 ±15%		
	Dielectric						70
2	VDD, GND					1/2	
	Dielectric						80
3	DQ	0.10	50 ±10%	0.10/0.10	83 ±15%	1/2	
	Address	0.075	55 ±10%	0.075/0.10	93 ±15%		
	Dielectric						420
4	VDD					1/2	
	Dielectric						80
5	Address/CK	0.075	55 ±10%	0.075/0.10	93 ±15%	1/2	
	Address/CK	0.15	40 ±10%	0.15/0.10	70 ±15%	1/2	
	Dielectric						420
6	Address	0.075	55 ±10%	0.075/0.10	93 ±15%	1/2	
	Address	0.15	40 ±10%	0.15/0.10	70 ±15%		
	Dielectric						80
7	VDD,GND					1/2	
	Dielectric						70
8	DQ	0.1	50 ±10%	0.10/0.10	83 ±15%	1/3 + Plating	
	Address/CK	0.075	55 ±10%	0.075/0.10	93 ±15%		
	Address/CK	0.15	40 ±10%	0.15/0.10	70 ±15%		

Proposed

The recommended construction and impedances can be found in the PCB Fabrication Table. The values in the table were used in the simulations during development and in the initial DIMMs used to verify operation. Deviations should be kept to a minimum.