Preliminary publication of JEDEC Semiconductor Memory Ballot

This Ballot was developed by JEDEC Committee JC-45 and approved by the JEDEC Board of Directors. It is published here in preliminary form, prior to being integrated into JEDEC Standard JESD21C and published in final form.

Title of Ballot: Proposed Annex for DDR4 UDIMM, R/C B

Council Ballot Number: JCB-13-062

Committee Ballot Number: 45.3-13-331

Committee Item Number: 2231.05

Date of Council Approval: Nov 2013

Background: This proposal was balloted as JC-45.3-13-331 on August 12, 2013 and expired on September 4, 2013. The voting results were reported at the September, 2013 JC-45.3 Committee meeting at which time the ballot was approved for Board of Directors submittal..

Annex B - Raw Card B

DDR4 Unbuffered DIMM Design File

Raw Card	Applicable Design File	Applicable BOM
B0	PC4-UDIMM_V070_RC_B0_20130802.brd	PC4-UDIMM_V070_RC_B0_20130802-Bom.txt
Note: “Reference” design file updates will be released as needed. This DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only. In these cases the design files will not be updated.		

Module Configuration

DIMM		SDRAM		# of SDRAM die	# of Package Ranks	# of Address bits row/col	MO-309 variation
Maximum Capacity	Organization	Die Density	Organization				
4GB	512Mx64	2Gbit	256M x 8	16	2	14/10[1]	AAxA
8GB	1Gx64	4Gbit	512M x 8	16	2	15/10[1]	AAxA
16GB	2Gx64	8Gbit	1G x 8	16	2	16/10[1]	AAxA
32GB	4Gx68	16Gbit	2G x 8	16	2	17/10	AAxA
1. Address A16 is the highest address bit used based on it being multiplexed with RAS_n.							

SDRAM Configuration

Supported DRAM Outline (Width x Length) max.	# of Banks in SDRAM BA/BG	SDRAM Package Type	Package Type	MO-207 variation
10.5 x 13.0	2/2	78 Ball FBGA	SDP	DW-z
Note: SDP is a single die per package				

Supported Speeds

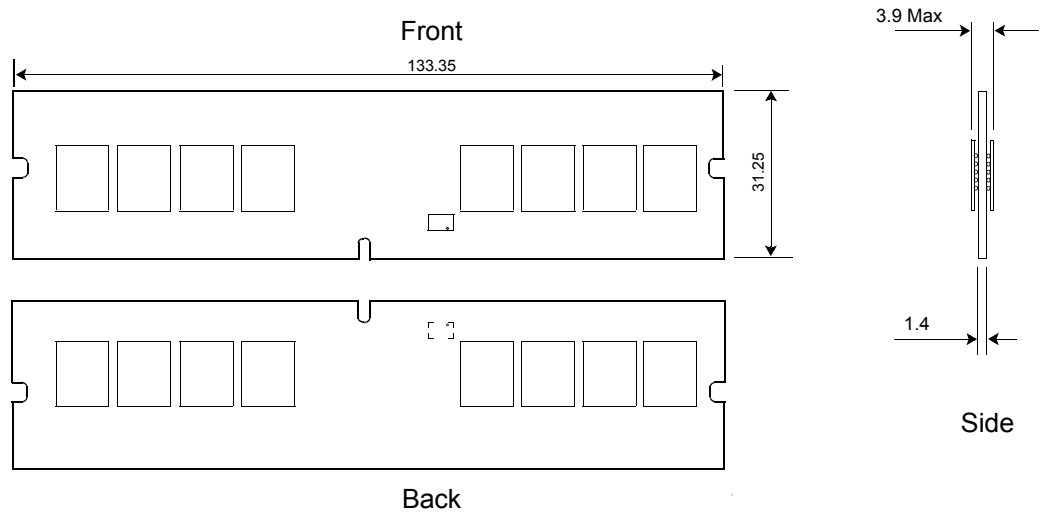
Raw Card	Speed	PC4-1333	PC4-1600	PC4-1866	PC4-2133	PC4-2400	PC4-2666	PC4-3200	Notes
B0	DDR4	X	X	X	X				1, 2
B0	DDR4L								1, 2
Note 1: X reflects speed grades approved from previous ballots. Note 2: P denotes speed grades being proposed for this most recent ballot									

Design Deviations

1. Clock mismatch at last SDRAM is 0.5 mm. Design Specification requirement is 0.2 mm.

Proposed

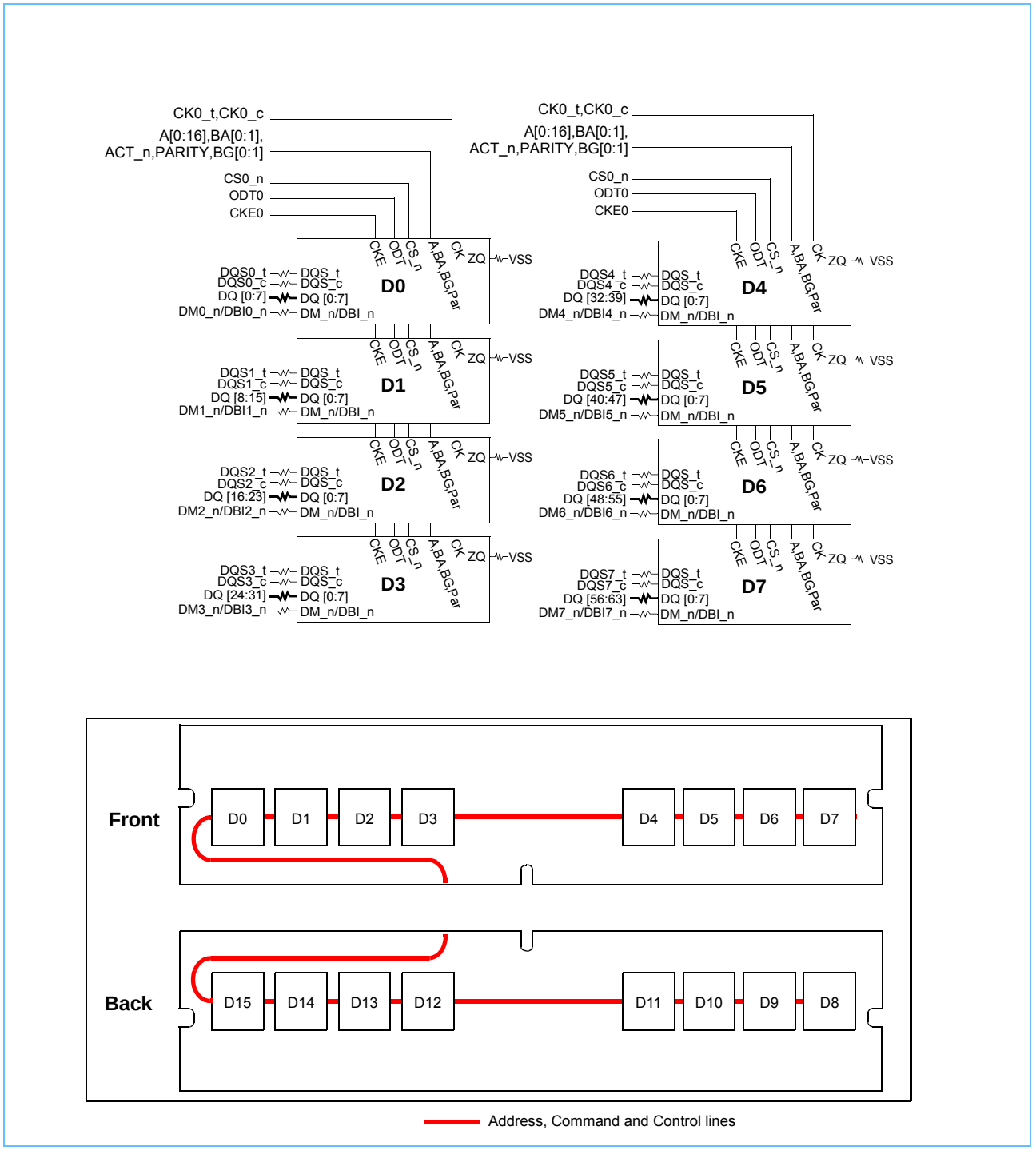
General Layout



Note 1: Refer to MO-309 for more detailed information.
Note 2: Variation is AAxA (A Module height, A Module thickness, x plating, A Key Position).

Functional Block Diagram

x64 DIMM, populated as two physical ranks of x8 DDR4 SDRAMs (Part 1 of 2)

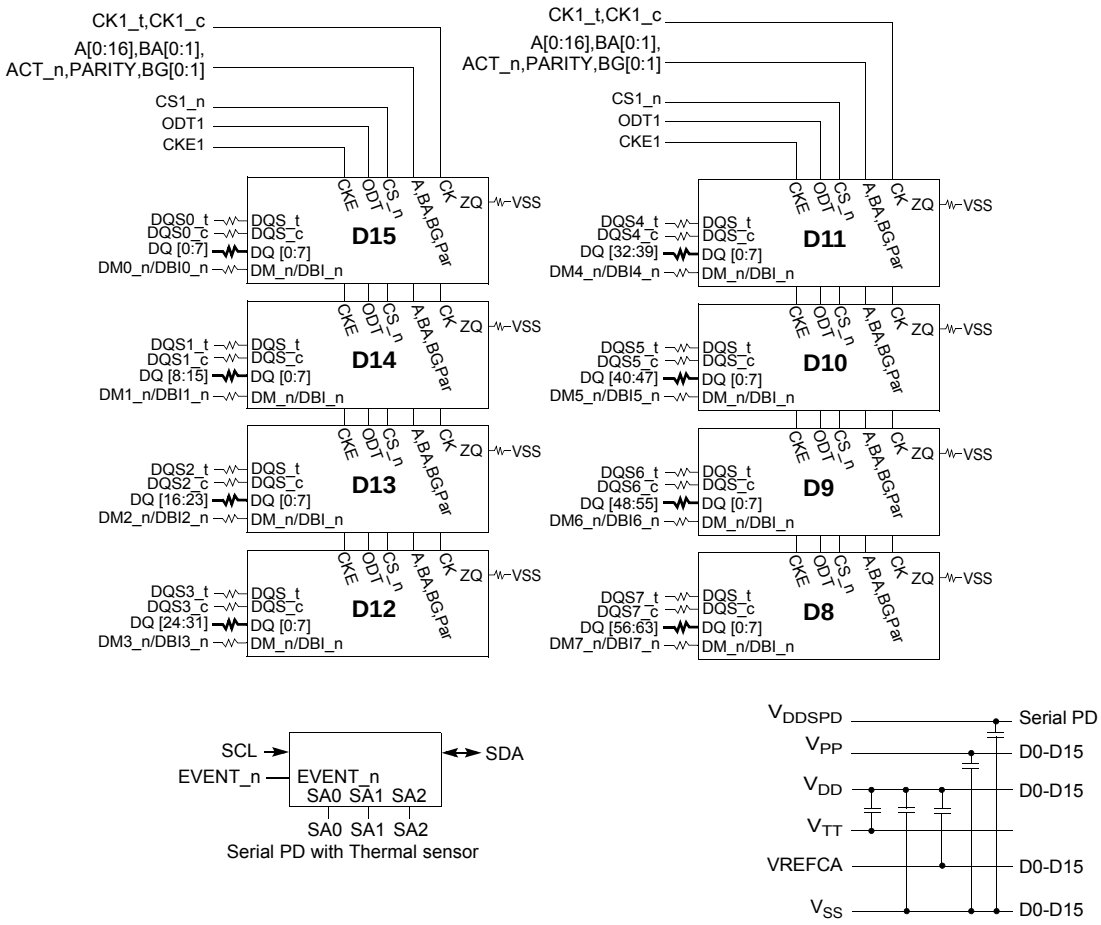


Proposed

Note 1: Unless otherwise noted, resistor values are 15Ω ± 5%.
Note 2: ZQ resistors are 240Ω ± 1%. For all other resistor values refer to the appropriate wiring diagram.

Functional Block Diagram

x64 DIMM, populated as two physical ranks of x8 DDR4 SDRAMs (Part 2 of 2)



Note 1: Unless otherwise noted, resistor values are 15Ω ± 5%.
Note 2: ZQ resistors are 240Ω ± 1%. For all other resistor values refer to the appropriate wiring diagram.
Note 3: For part 2 of 2 the DQ resistors are shown for simplicity but are the same physical components as shown on part 1 of 2.
Note 4: EVENT_n is wired on this design. A standalone SPD may be used as well. No wiring changes are required.

Input Loading and Test Points

Input Loading

Signal Names	Input to Device	Loads
CK0_t, CK0_c	SDRAMs	8
CK1_t, CK1_c	SDRAMs	8
RESET_n	SDRAMs	16
CKE0, CKE1, ODT0, ODT1	SDRAMs	8
Ax, BAx, RAS_n, CAS_n, WE_n, ACT_n, PARITY	SDRAMs	16
CS0_n, CS1_n	SDRAMs	8
DQ, CB, DQS_t, DQS_c	SDRAMs	2
DMx_n/DBIx_n	SDRAMs	2
SCL,SDA,SA[2:0], EVENT_n	SPD	1

Test Point Locations

Signal Group	Signal	Signal locations
Address/Command/ Control/PARITY	All	Termination resistors on the end of the module
DQ, CB, DM_n, DBI_n	All	15 Ohm resistors
DQS_t, DQS_c	All	15 Ohm resistors
Clock	All	Termination resistors
Note 1: Refer to the registration package for additional test point information.		

DQ Map for CRC

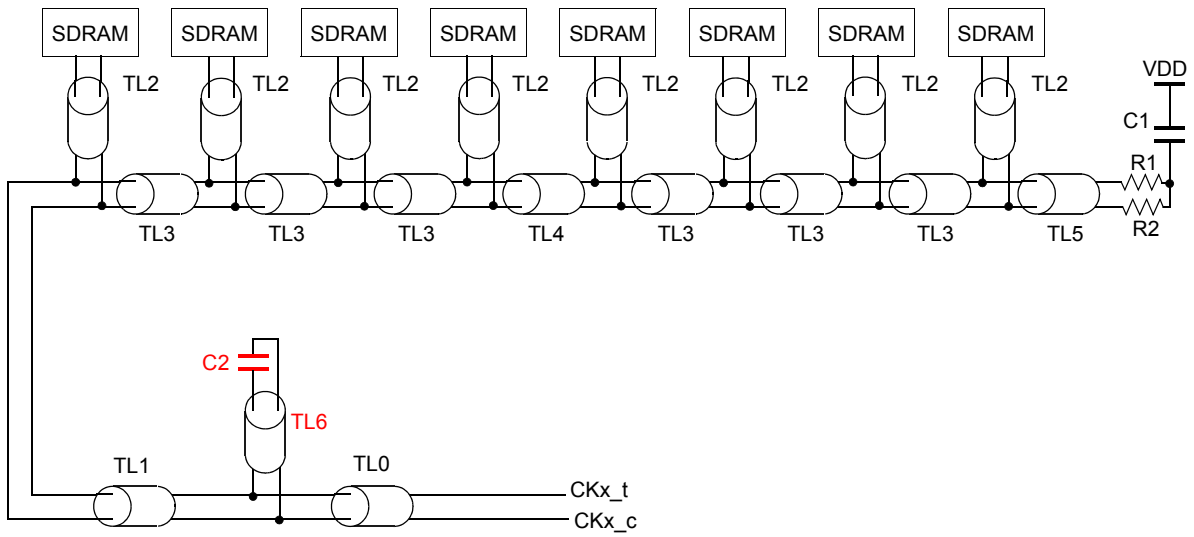
See Common section of the DDR4 UDIMM Design Specification for information on interpreting the DQ Mapping table.

SPD Values for DQ Mapping

DQ Bits as defined by connector	SPD Byte (Decimal)	SPD Value (Hex)	DQ Bits as defined by connector	SPD Byte (Decimal)	SPD Value (Hex)
DQ0, DQ1, DQ2, DQ3	60	16	DQ32, DQ33, DQ34, DQ35	70	2B
DQ4, DQ5, DQ6, DQ7	61	36	DQ36, DQ37, DQ38, DQ39	71	0C
DQ8, DQ9, DQ10, DQ11	62	16	DQ40, DQ41, DQ42, DQ43	72	2B
DQ12, DQ13, DQ14, DQ15	63	36	DQ44, DQ45, DQ46, DQ47	73	0C
DQ16, DQ17, DQ18, DQ19	64	16	DQ48, DQ49, DQ50, DQ51	74	2B
DQ20, DQ21, DQ22, DQ23	65	36	DQ52, DQ53, DQ54, DQ55	75	0C
DQ24, DQ25, DQ26, DQ27	66	16	DQ56, DQ57, DQ58, DQ59	76	2B
DQ28, DQ29, DQ30, DQ31	67	36	DQ60, DQ61, DQ62, DQ63	77	0C
	68	00			
	69	00			

Clock Net Structure

Net Structure Routing for Clock to SDRAM Loads



Trace Lengths for Clock to SDRAM load Net Structures

Signal	TL0 MS	TL1 SL	TL2 (MS)	Length to First SDRAM[2] TL0+TL1+TL2 with Via Compensation Equivalent SL	TL3 SL	TL4 SL	Length to Last SDRAM[2] TL0+TL1+TL2 +TL3's+TL4 with Via Compensation Equivalent SL	TL5 MS+SL	TL6 MS	R1, R2 Ω	C1 (uF)	C2 (pF)	Notes
CK0_t	6.6	102.5	1.4	110.0	18.5	34.1	255.4	19.7	1.5	36 ± 5%	0.01	0	1
CK0_c	6.2	102.6	1.4	110.0	18.5	34.1	255.2	20.8	1.5				1
CK1_t	6.8	101.3	1.4	110.2	18.5	34.1	254.9	14.8	1.5				1
CK1_c	6.2	101.9	1.4	110.2	18.5	34.1	255.3	14.0	1.5				1

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.1millimeters.
2. Equivalent SL is defined by MS (Microstrip) sections being adjusted by dividing by 1.10. Any imbalance in vias is compensated as 2 times the Z axis length of the travelled path.

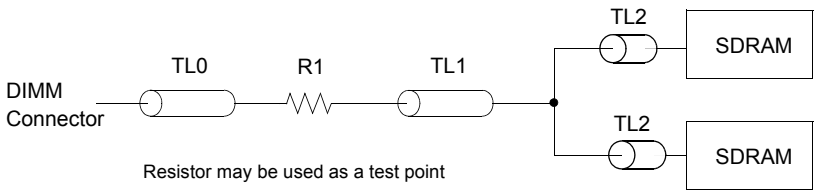
Proposed

Data Net Structure - DQ, DQS_t, DQS_c, DM_n/DBI_n.

This group includes DQ[0:63], DQS[0:7]_t, DQS[0:7]_c, DM[0:7]_n/DBI[0:7]_n.

Recommend delays for all nets, as described in the following tables.

Net Structure for DQ, DQS_t, DQS_c, DM_n/DBI_n



Trace Lengths for DQS[0:7]_t, DQS[0:7]_c, DQ[0:63], DM[0:7]_n/DBI[0:7]_n

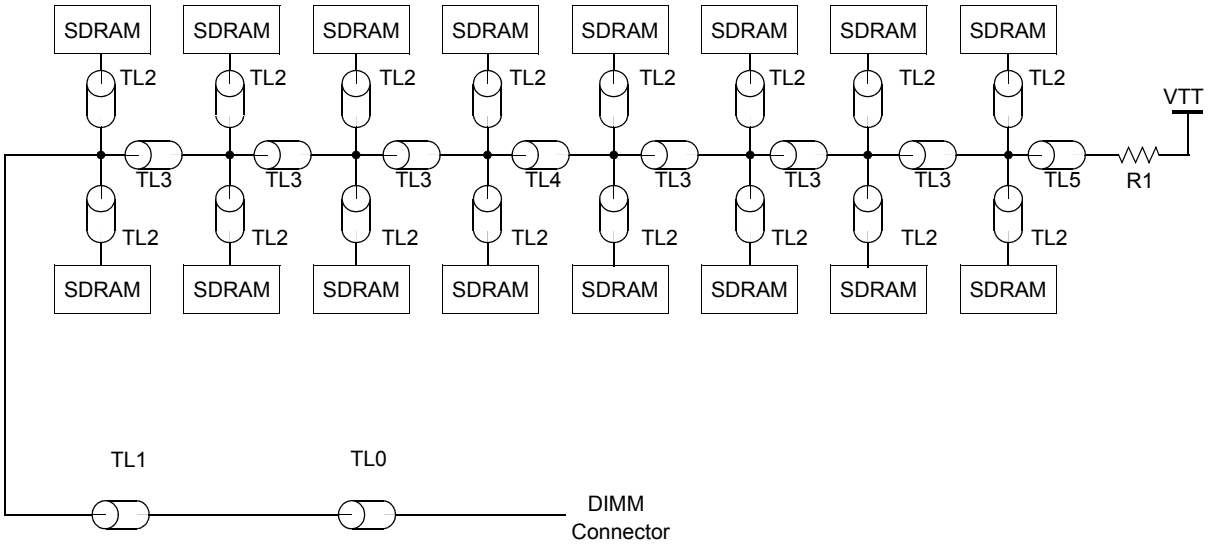
DQ Signals	TL0		TL1		TL2		TL0+TL1+TL2 + Via Compensation Equivalent SL		R1 (Ohms)	Notes
	Min	Max	Min	Max	Min	Max	Min	Max		
DQS0_t, DQS0_c, DQ[0:7], DM0_n/DBI0_n	3.2	4.7	14.4	18.2	0.6	1.8	21.3	21.8	15 ± 5%	1, 2
DQS1_t, DQS1_c, DQ[8:15], DM1_n/DBI1_n	2.9	4.4	21.0	25.5	0.6	1.8	28.3	29.0	15 ± 5%	1, 2
DQS2_t, DQS2_c, DQ[16:23], DM2_n/DBI2_n	2.9	4.4	18.6	22.7	0.6	1.8	25.2	26.0	15 ± 5%	1, 2
DQS3_t, DQS3_c, DQ[24:31], DM3_n/DBI3_n	3.1	5.7	22.6	28.0	0.6	1.8	30.6	31.3	15 ± 5%	1, 2
DQS4_t, DQS4_c, DQ[32:39], DM4_n/DBI4_n	3.1	4.6	21.2	25.4	0.6	1.8	28.5	29.1	15 ± 5%	1, 2
DQS5_t, DQS5_c, DQ[40:47], DM5_n/DBI5_n	3.0	5.9	17.2	22.5	0.6	1.8	25.6	26.3	15 ± 5%	1, 2
DQS6_t, DQS6_c, DQ[48:55], DM6_n/DBI6_n	2.9	4.3	20.3	24.4	0.6	1.8	27.0	27.6	15 ± 5%	1, 2
DQS7_t, DQS7_c, DQ[56:63], DM7_n/DBI7_n	3.1	5.9	12.4	17.8	0.6	1.9	20.6	21.4	15 ± 5%	1, 2

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.1 mm.
2. Any MS (Microstrip) sections are converted to equivalent SL (Stripline) by dividing by 1.10. Any imbalance in vias is compensated as 2 times the Z axis length of the travelled path.

Proposed

Address and Command Net Structure Routing

A[0:16], BA[0:1], BG[0:1], ACT_n, PARITY



Trace Lengths Address and Command Net Structures

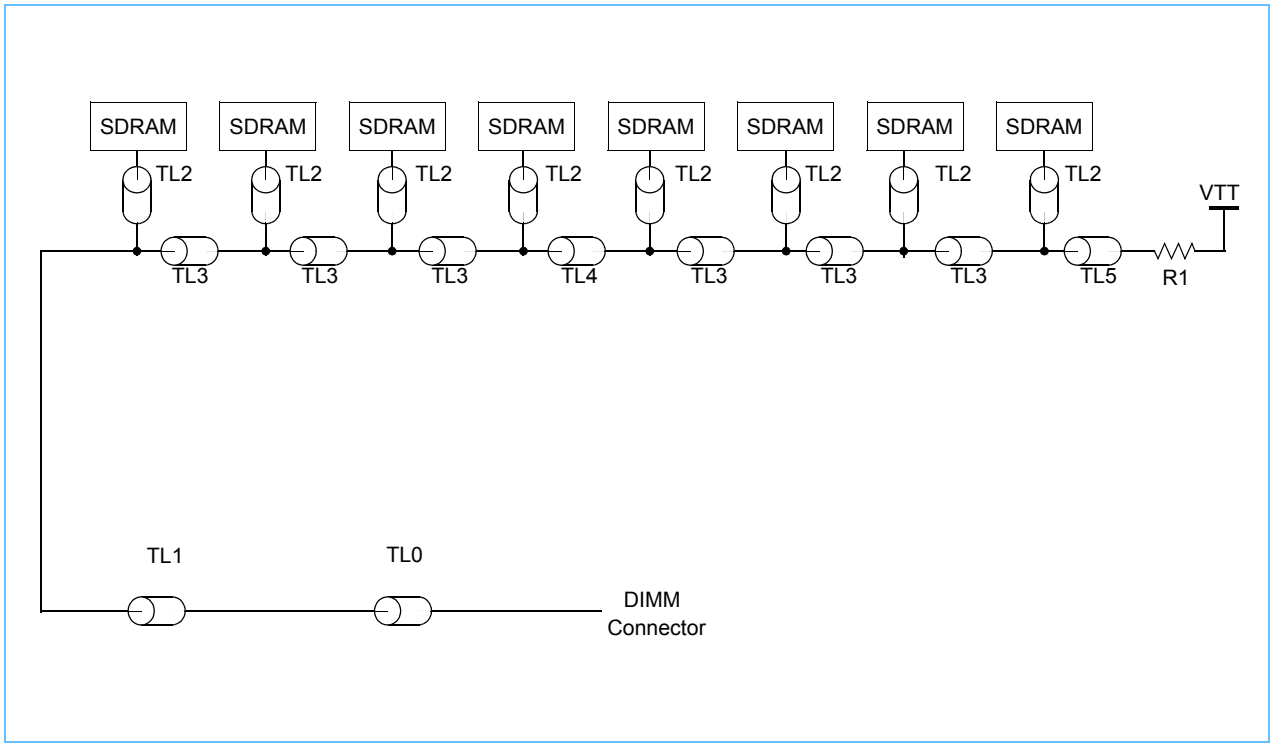
	TL0 MS	TL1 SL	TL2 MS	First SDRAM TL0+TL1+TL2 + Via Compensation Equivallent SL	TL3 SL	TL4 SL	Last SDRAM TL0+TL1+TL3's+TL4+TL2 +Via Compensation Equivalent SL	TL5	R1 Ohms	Notes
Min	1.7	74.5	0.6	107.6	13.2	34.0	227.7	17.8	39 ± 5%	1, 2, 3, 4, 5
Max	35.5	104.1	3.2	108.2	13.5	34.4	228.7	23.1		

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.1 millimeter.
2. Any MS (Microstrip) sections in are converted to equivalent SL (Stripline) by dividing by 1.10. Any imbalance in vias is compensated as 2 times the Z axis length of the travelled path.
3. For the TL2 length only the TOP layer length is included.
4. This design uses address mirroring.
5. TL5 lengths are not required to be met.

Proposed

Control Net Structure Routing

CS[0:1]_n, CKE[0:1], ODT[0:1]



Trace Lengths of Control Net Structures

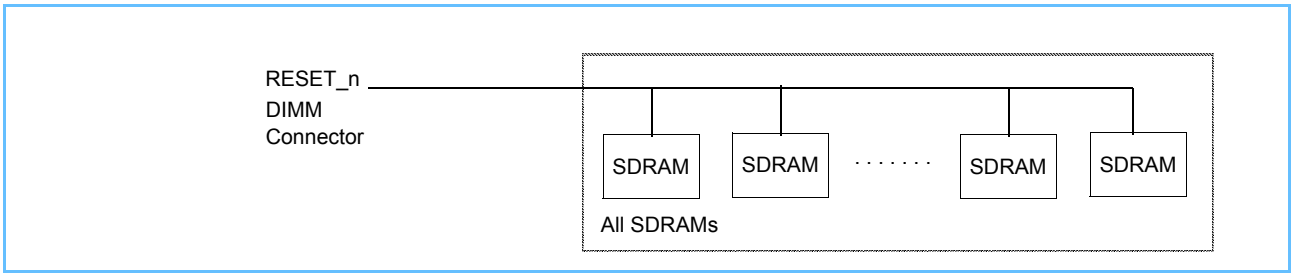
	TL0 MS	TL1 SL	TL2 MS	First SDRAM TL0+TL1+TL2 + Via Compensation Equivalent SL	TL3 SL	TL4 SL	Last SDRAM TL0+TL1+TL3's+TL4+TL2 +Via Compensation Equivalent SL	TL5 SL	R1	Notes
Min	3.3	76.2	1.1	110.1	18.4	34.0	254.9	14.7	39 ± 5%	1, 2, 3
Max	33.7	104.6	1.4	110.4	18.6	34.2	255.5	18.8		

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.1 millimeters.
2. Any MS (Microstrip) sections in are converted to equivalent SL (Stripline) by dividing by 1.10. Any imbalance in vias is compensated as 2 times the Z axis length of the travelled path.
3. TL5 lengths are not required to be met.

Proposed

RESET_n and Event_n Net Structures

RESET_n Net



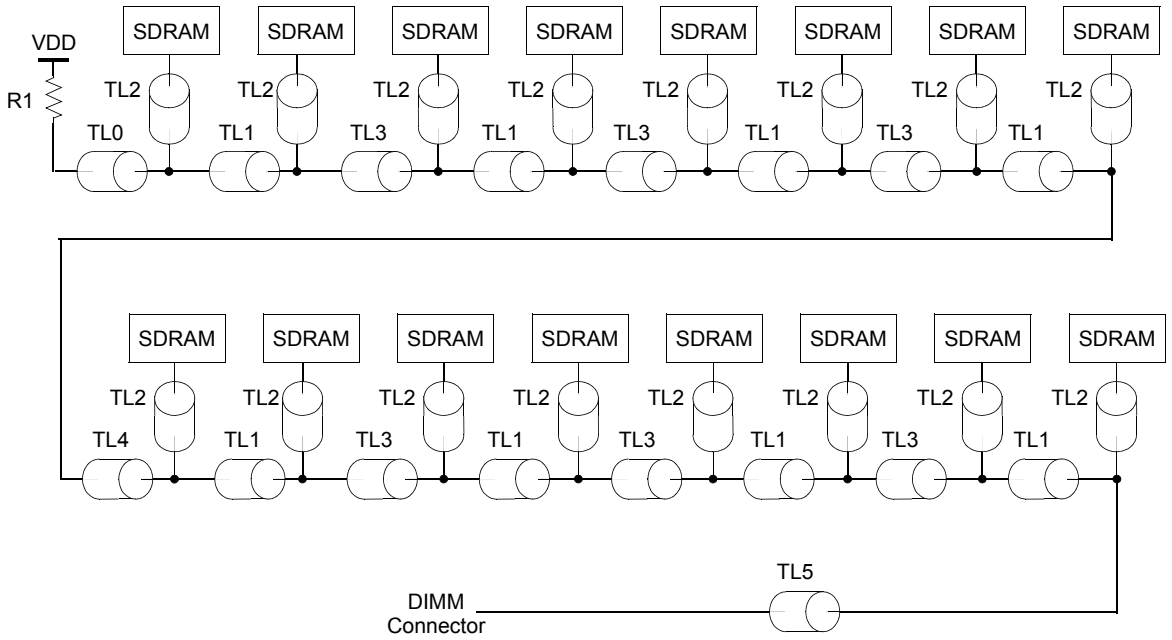
RESET_n Net Total Length

Total Net Length	
RESET_n	207

1. Total length of all traces together (in millimeters) is specified and must be kept within a tolerance of ± 10%.
2. RESET_n routing follows the address routing. Individual lengths are not specified.

ALERT_n

ALERT_n Net Structure



Proposed

Trace Lengths of ALERT_n Net Structure

TL0	TL1	TL2	TL3	TL4	TL5	R1 (Ohms)	Notes
5.9	8.6	0.6	5.0	23.0	110.9	51 ± 5%	1

1. All distances are given in millimeters and must be kept within a tolerance of ± 3.0 mm.

Cross Section Recommendations

PCBs should contain solid ground plane and power plane layers as far as possible. Minimum trace width allowed is 0.075 mm.

The PCB edge connector contacts shall be gold plated.

Any exceptions to these design rules has been identified in the front of this annex.

PCB Fabrication Table

Layer	Layer Description	Single-ended Impedances		Differential Impedances		Copper oz	Dielectric Thickness (um)
		Trace Width (mm)	Impedance (Ohms)	Trace Width/Spacing (mm / mm)	Impedance (Ohms)		
1	GND						
	DQ	0.10	50 ±10%	0.10 / 0.10	83 ±15%	1/2 + Plating	
	Address/CK	0.075	55 ±15%	0.075 / 0.10	93 ±15%		
	Address/CK	0.15	40 ±15%	0.15 / 0.10	70 ±15%		
	Dielectric						70
2	VDD/VSS					1/2	
	Dielectric						80
3	Address/CK	0.075	55 ±15%	0.075 / 0.10	93 ±15%	1/2	
	Address/CK	0.15	40 ±15%	0.15 / 0.10	70 ±15%		
	Dielectric						420
4	Address	0.075	55 ±15%	0.15 / 0.10	70 ±15%	1/2	
	Address	0.15	40 ±15%				
	Dielectric						80
5	VDD					1/2	
							420
6	Address/CK	0.075	55 ±15%	0.075 / 0.10	93 ±15%	1/2	
	Address	0.15	40 ±15%				
	DQ	0.10	50 ±10%	0.10 / 0.10	83 ±15%		
							80
7	VDD/VSS					1/2	
	Dielectric						70
8	VPP/GND					1/2 + Plating	
	Address/CK	0.15	40 ±15%	0.15 / 0.10	70 ±15%		
	Address/CK	0.075	55 ±15%	0.075 / 0.10	93 ±15%		
	DQ	0.10	50 ±10%	0.10 / 0.10	83 ±15%		

Proposed

The recommended construction and impedances can be found in the PCB Fabrication Table. The values in the table were used in the simulations during development and in the initial DIMMs used to verify operation. Deviations should be kept to a minimum.