The Programmable Solutions Company®

Stratix II Memory Board II

Layout Guidelines
Rev 0.4

High-Speed End Applications
08/24/2004

REVISION HISTORY

DATE	REV	Comments
06/29/04	0.1	Created
07/27/04	0.2	Added figure 4-4,4-5. Removed feedback signals.
08/06/04	0.3	Added silkscreen info for jumpers and switches, Changed thickness back to 62-mil
08/24/04	0.4	Added section 6. Updated figures.

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1. Form Factor

1.1. Overall Form Factor

S2MB2 should be approximately 7” x 8.5”.

1.2. Keepouts

Board-Edge shall be component-free for 0.125”
Edge-Components are an exception to this and are covered in the edge components section.

1.3. Tooling and Mounting Holes

Four 0.125” plated mounting holes shall be placed in the four corners of the board (0.250” pad)
One 0.125” plated mounting hole shall be placed between the DIMM and Stratix II (0.250” pad)

1.4. Breakaways

None are currently planned.

2. Construction

PCB shall use high-temp FR4
Controlled Impedance
- – All signal planes to be 50-ohms single ended impedance +/- 10%
- – All signal planes to be 100-ohms differential impedance +/- 10%

12-layer, 62-mil finished PCB thickness

2.1. Geometries

2.1.1. Trace Geometries

5 mil trace (min)
5 mil space (min)

2.1.2. Via Geometries

10 mil drill (min, typ)
TEST VIA to have 30-mil pad on bottom-side
Special STAR_VIA components are special test VIAs actually placed in the schematic
-These vias are used to break-out multiple loaded address/control signals from a datapath signal for use in special length-matching requirements. See critical routing section for more details.

2.2. Stackup

2.2.1. Overview

8 Routing / 8 Power

1	**Signal**
2	**GND**
3	**Signal**
4	**Signal**
5	**1.2V**
6	**Signal**
7	**Signal**
8	**3.3V**
9	**Signal**
10	**Signal**
11	**Split Power (3 planes)**
12	**Signal**

2.2.2. Signal Planes

2.2.3. Power Planes

The following power signals must be routed as planes:

1) GND
2) 3.3V
3) 1.2V

The following power signals should be routed in a single split plane with 20-mil gaps of separation:

4) 1.8V_DIMM
5) 1.8V_DDR2
6) VDD_QDRII_IO

The approximate split is shown in Figure 2-1 below. See the Placement Diagram for more details on top-side components.

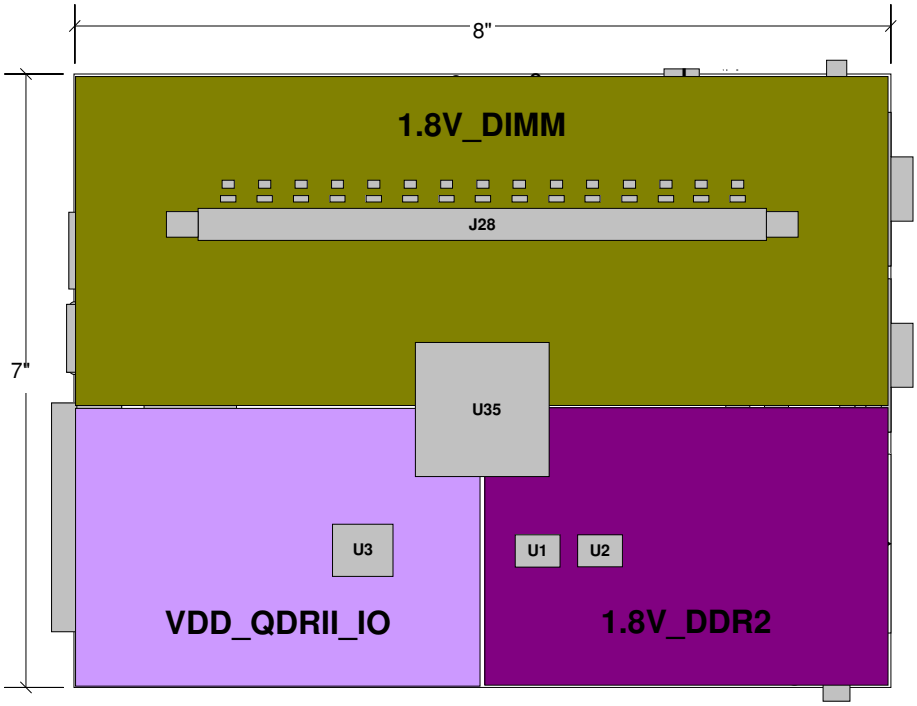


Figure 2-1 Split Plane Architecture

The following power signals should be routed as 750-mil power traces on signal layers:

7) 1.8V

The following power signals should be routed as islands or 250-mil power traces on signal layers:

8) VDD_QDRII_INT
9) 0.9V_DIMM
10) 0.9V_DDR2
11) VTT_QDRII
12) DC_INPUT

The following power signals should be routed as islands or 100-mil power traces on signal layers:

13) VCC_PLL
14) 3.3V_OSCA
15) 3.3V_OSCB
16) 3.3V_CLKA
17) 3.3V_CLKB
18) 1.8V_CLKB
19) GND_PLL

Aggregate trace width is the main consideration for the 250-mil traces. Use top-bottom layers to double up two 125-mil traces with some via stitching where needed.

VCC_PLL power traces can be 100-mils upon entering the BGA via grid. The traces that snake around the outside of the Stratix II BGA should try to keep 100-mil thickness.

2.3. In-Circuit Test Requirements

1. 100% breakout to a minimum of 1 test via per net
    - Through-hole component pin counts as a test via
    - Exceptions to this are unused BGA pins (no via required)
    - Further exceptions to be approved by the responsible design engineer
2. Test VIA defined in via geometries section.

2.4. Fiducials

1. Two fiducials to be placed on opposite corners of PCB, top AND bottom side.
2. All fine-pitch components to have at least one fiducial per instance (see 3.2).

3. Component Placement

3.1. General Placement Rules

3.1.1. Surface-Mount

BGA to Surface-mount must have minimum 150-mil clearance.

3.1.2. Through-Hole

Through-hole to Surface-mount on bottom side clearance must be greater than 200-mils.

3.2. Fine Pitch Components

These components should have local fiducials and silkscreen pin markings every 10 pins with a pin number label on every corner for regular QFP/TSOP pinned-packages and labels on every row and column for BGA packages.

No.	Component Name	Ref Des
1	EP2S60F1020	U13
2	EPM7256AE	U16
3	EPM1270	U17
4	MT47H16M16	U28,U29
5	CY7C1313V18	U30,U36
6	ICS85214	U23
7	LAN91C111	U10
8	AM29LV128	U35
9	LTC2901	U25
10	LTC2418	U22

There will be an option to load the EPM7256AE (Max) or the EPM1270 (Max II) on this board. The Max II will be an 256 FBGA package and the footprint will be inside the T144 outline for the Max. This was done to save board space.

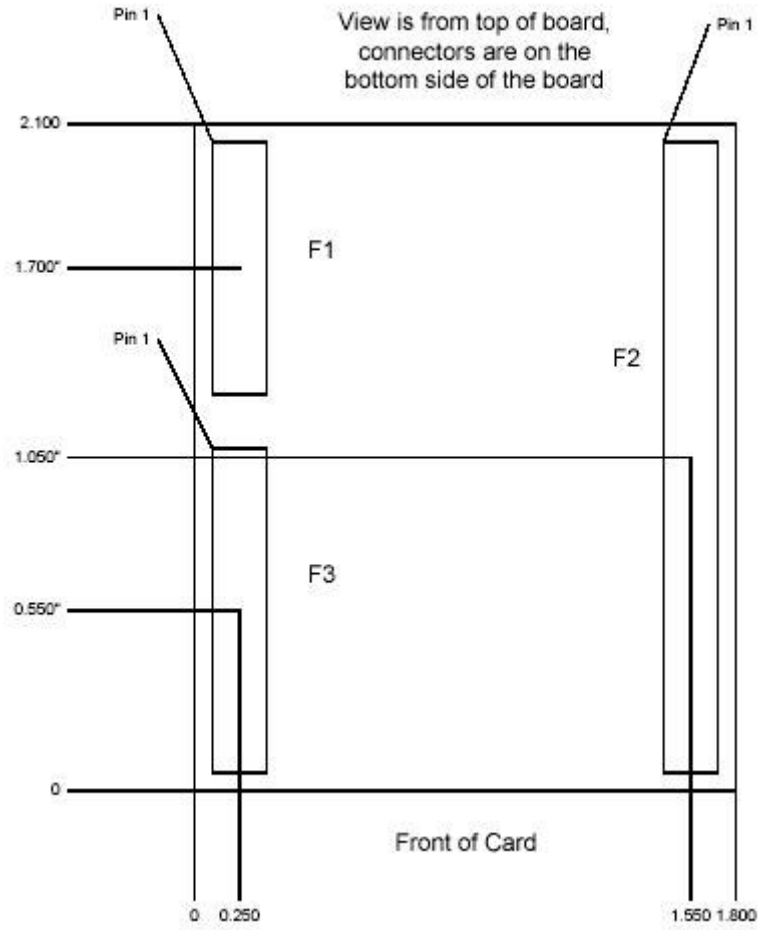
3.3. Special Components

3.4. Connectors

3.4.1. Altera Daughter Card "PROTO1" (J33,J42,J43)

The 3.3V Altera Daughter Card interconnect is made up of three 100-mil headers. These are arranged in two columns. The two columns are made up of one combo 2x7 + 2x10 (J42 + J43 respectively) and the other is made up of a single 2x20 (J33).

These are to be placed according to the *placement drawing*. Relative placement is according to the drawing below. The "front of card" as shown is to align with the PCB edge.



3.4.2. Banana Jacks (J3-J9, J29-J32)

The banana jacks shall be placed no closer than 0.500" center-to-center.

3.4.3. RS-232 (J12, J19)

The RS-232 connectors should be placed with a slight overhang to the PCB edge. The faceplate of the connectors should be either flush to the PCB edge of hand over up to 1/8" from the PCB edge.

3.4.4. RJ-45 (J21)

The RJ-45 connector should be placed on the PCB edge with a 1/8" overhang.

3.4.5. Byte Blaster Header (J17)

The Byte-Blaster connector should placed on the PCB edge with a 1/8" overhang.

3.4.6. JTAG Expansion Connectors (J1, J54)

The JTAG Expansion Connectors should be placed on the PCB edge with an approximate 1/8" overhang. They should be able to mate with each other if two Stratix II Memory Boards were connected edge-to-edge.

3.4.7. DC Input Connector (J2)

The DC Input Connector should be placed on the PCB edge with a 1/8" overhang.

3.5. Test Points

The following test points are through-hole 25-mil square-pin posts. They should have a silkscreen outline around the base plastic. The geometry for these should be TP_060SQ040.

TP3, TP4, TP5, TP6, TP8, TP10–TP26

The following test points are special vias that are exposed on the top-side and bottom-side with a 30-mil pad:

STAR_VIA

3.6. Height Restrictions

Anything placed within the outline of the Altera Daughter Card (see 3.4.1) must be no taller than 1/4" tall due to the daughter cards that plug into this set of connectors. The overall height of the adjoining parallel PCB that would plug into this interface is ½" (surface-to-surface) but we must allow for daughter card components on the bottom-side of up to 3/16" and an air gap of 1/16". Placement height within the interface outline must limited to 3/16".

3.7. Placement Drawings

3.7.1. Top Side

The figure below should be used as reference only. The figure is not drawn to scale and only shows approximate placement of parts on S2MB2.

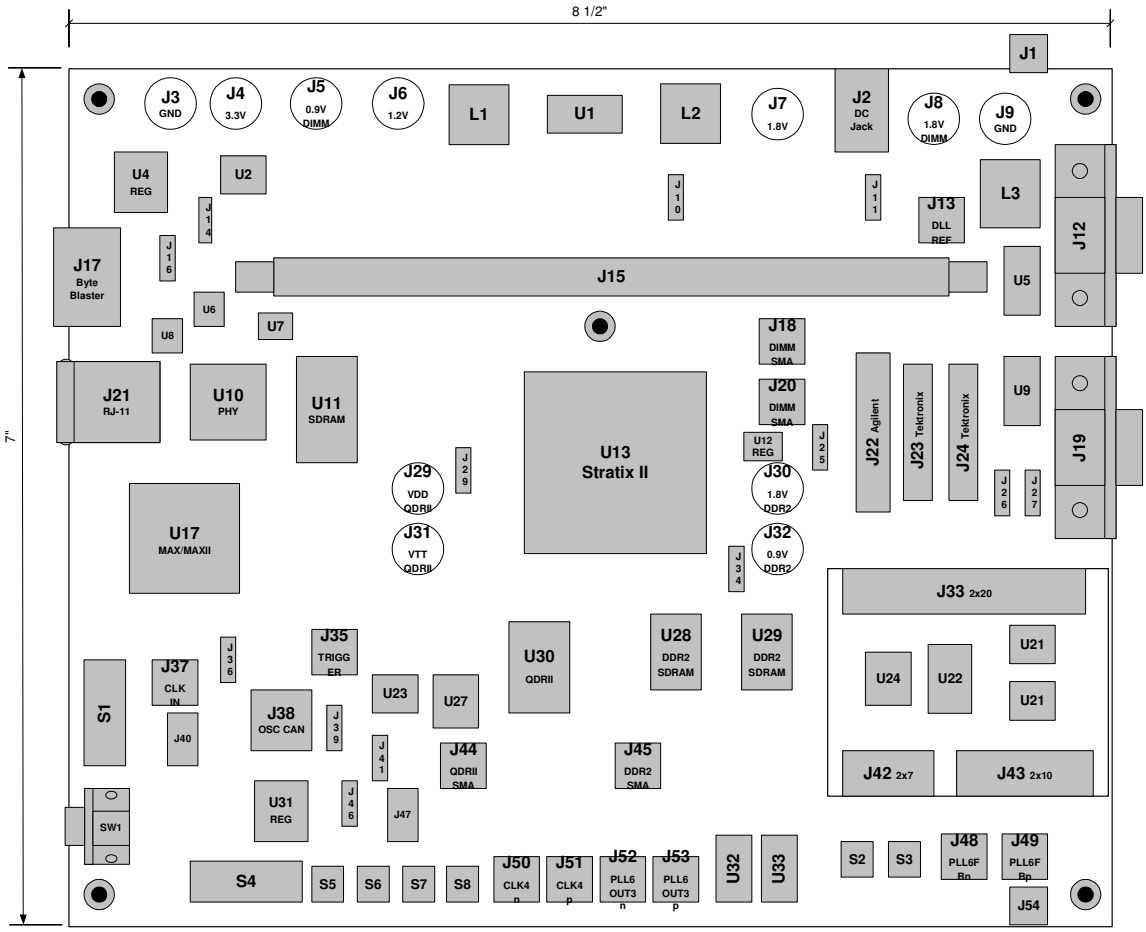


Figure 3-1

3.7.2. Bottom Side

No bottom-side drawing will be supplied. Mostly passives will be placed on the bottom such as decoupling caps and resistors. The only potential active components for the bottom are the Flash (U35), one of the two SRAM components (either U11 or U34) in a clamshell mount, and one of the two QDRII SRAM devices (U36) in a clamshell mount. This will depend on actual placement with real part sizes and keepouts. Other bottom-side components must be approved by the responsible engineer.

3.7.3. Switching Power Supply

Figure 3-2 shows an approximate placement for major components within the dual-output switching power supply used to create both 1.2V and 1.8V controlled by U1.

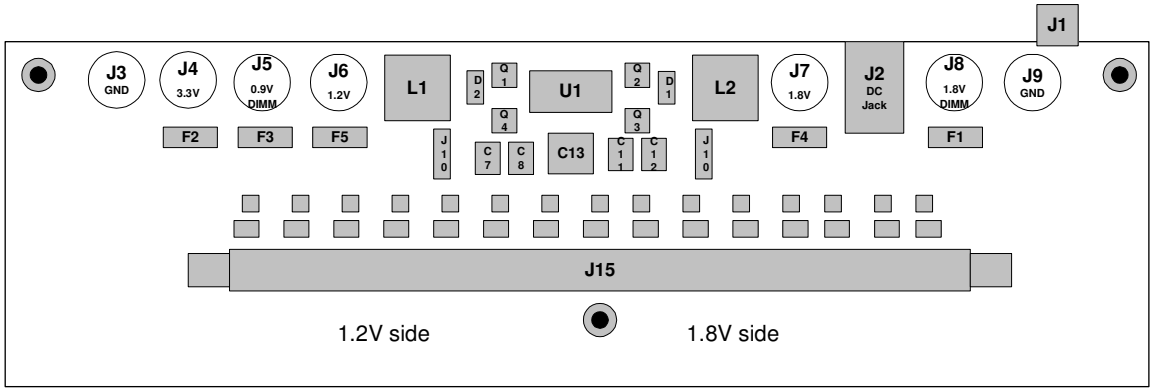


Figure 3-2

Figure 3-3 shows an approximate placement for top-layer copper pour regions between these components. For ties between these poured islands and a plane there must be multiple vias used (at least 6 if not 8 or 10) for high-current and low resistance and inductance.

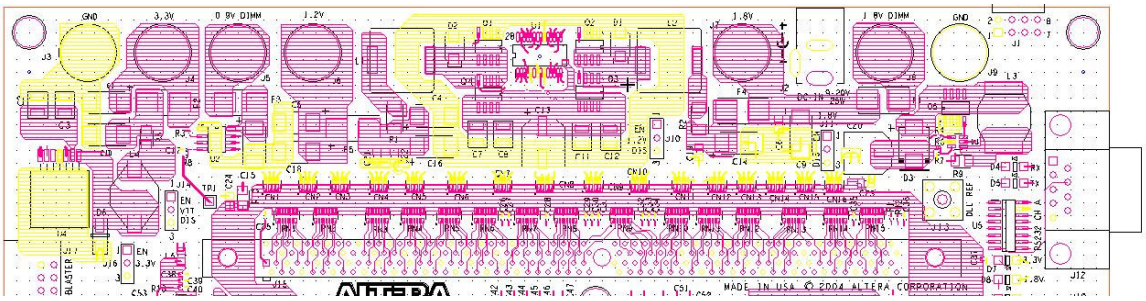


Figure 3-3

4. Routing Rules

4.1. General

1. Use 45 degree angles (no 90 degree corners)
2. No T-junctions greater than 250 mils
3. No T-junctions for critical nets or clocks (see critical traces section) unless otherwise specified.

4.2. Power Traces

The following power signals should be routed as islands or 250-mil power traces:

1) 0.9V_DIMM
2) 0.9V_DDR2
3) VTT_QDRII
4) DC_INPUT

The following power signals should be routed as islands or 100-mil power traces:

5) VCC_PLL
6) 3.3V_OSCA
7) 3.3V_OSCB
8) 3.3V_CLKA
9) 3.3V_CLKB
10) 1.8V_CLKB

See the power section for other potential notes on power traces.

4.3. Clocks

The following signals are designated as clocks.

-They are to be routed on inner layers with outer-layer run lengths being held to under 500 mils.
-These signals should maintain a 10-mil spacing from other nets.
-Differential clocks should maintain a length-matching between P and N signals of +/- 15 mils.
-Differential clocks with SMAs should route as a Diff Pair and break-out to SMAs right at the connectors.

Some termination resistor placement is mentioned below as well on a per-clock basis.

4.3.1. Oscillators

1)	OSCA	33.333 MHz	Oscillator to be close to destination pin
2)	OSCB	100.000 MHz	Oscillator to be close to destination pin
3)	CLK_25MHz	25.000MHz	Oscillator to be close to destination pin

4.3.2. SMA

4)	CLKB_SMA	350 MHz MAX	R142 close to U23 (buffer)
5)	CLK4_P	350 MHz MAX	Diff Pair (P/N) input to U13
	CLK4_N	350 MHz MAX	R134, R133 close to U13
6)	PLL6_FB_P	267 MHz MAX	Diff Pair (P/N) input to U13
	PLL6_FB_N	267 MHz MAX	
7)	PLL6_OUT0_P	267 MHz MAX	Diff Pair (P/N) output to SMAs
	PLL6_OUT0_N	267 MHz MAX	

4.3.3. Clock Buffers

8)	OSCA_TP	33.333 MHz	TP2,TP3 close to U7, buffer test point
9)	OSCA_PROTO1	33.333 MHz	R157,C366 close to J43
10)	OSCA_CPLD	33.333 MHz	R15 close to U7
11)	OSCA_CLK10	33.333 MHz	R16 close to U7
12)	CLKB_TP_P	100.000 MHz	Diff Pair (P) buffer test point to
	CLKB_TP_N	100.000 MHz	SMA close to R60 and U23
13)	OSCB_CLK5_P	100.000 MHz	Diff Pair (P/N) Stratix II inputs
	OSCB_CLK5_N	100.000 MHz	R137,R138 close to U13
14)	OSCB_CLK6_P	100.000 MHz	Diff Pair (P/N)
	OSCB_CLK6_N	100.000 MHz	R136,R135 close to U13
15)	OSCB_CLK12_P	100.000 MHz	Diff Pair (P/N)
	OSCB_CLK12_N	100.000 MHz	R97,R98 close to U13
16)	OSCB_CLK14_P	100.000 MHz	Diff Pair (P/N)
	OSCB_CLK14_N	100.000 MHz	R99,R100 close to U13

4.3.4. Memory Clocks

17)	DIMM_CK_P0	267 MHz	Diff Pair (P/N)
	DIMM_CK_N0	267 MHz	
18)	DIMM_CK_P1	267 MHz	Diff Pair (P/N)
	DIMM_CK_N1	267 MHz	
19)	DIMM_CK_P2	267 MHz	Diff Pair (P/N)
	DIMM_CK_N2	267 MHz	
20)	DIMM_SYNC_CLK	267 MHz	R122 close to U13, Core Re-Sync Clock
21)	DDR2_CK_P0	267 MHz	Diff Pair (P/N)
22)	DDR2_CK_N0	267 MHz	
23)	DDR2_CK_P1	267 MHz	Diff Pair (P/N)
24)	DDR2_CK_N1	267 MHz	
25)	DDR2_SYNC_CLK	267 MHz	Core Re-Sync Clock
26)	QDRII_K_P0	250 MHz	Single-ended
27)	QDRII_K_N0	250 MHz	Single-ended
28)	QDRII_K_P1	250 MHz	Single-ended
29)	QDRII_K_N1	250 MHz	Single-ended
30)	QDRII_CQ_P0	250 MHz	Single-ended
31)	QDRII_CQ_N0	250 MHz	Single-ended
32)	QDRII_CQ_P1	250 MHz	Single-ended
33)	QDRII_CQ_N1	250 MHz	Single-ended
34)	QDRII_SYNC_CLK	250 MHz	Core Re-Sync Clock

4.4. Critical Traces

4.4.1. DDR2 Devices

The following signals run between the DDR2 Devices (U28, U29) and the Stratix II FPGA (U13). Signals with similar names such as DDR2_A and DDR2_A_R are the same trace separated by a series resistor. In these cases the overall net length is actually the sum of the two nets. The address/command group signals are bussed to both devices. The remaining signals are point-to-point with the exception of some signals having series resistors.

Restrict routing layers for critical signals (those on the 3 high-speed memory interfaces) to internal layers only.

Address/Command Group

Address =	DDR2_A(15:0)	DDR2_A_R(15:0)
Bank Addr =	DDR2_BA(2:0)	DDR2_BA_R(2:0)
Command =	DDR2_RASn	DDR2_RASn_R
	DDR2_CASn	DDR2_CASn_R
	DDR2_WEn	DDR2_WEn_R

Control Group

Chip Selects =	DDR2_CSn(1:0)	DDR2_CSn_R(1:0)
Clock Enable =	DDR2_CKE	DDR2_CKE_R
On-Die Term Enable =	DDR2_ODT	DDR2_ODT_R

Data Group

Data =	DDR2_DQ(31:0)
Data Mask =	DDR2_DM(3:0)
Data Strobe =	DDR2_DQS(3:0)

Clock Group

Diff. Clocks =	DDR2_CK_P0	DDR2_CK_N0	(diff pair)
	DDR2_CK_P1	DDR2_CK_N1	(diff pair)

From the above signals a set of groups are made. Each group represents a byte of data and an associated clock and mask control. These will become match groups.

Byte Lane Groups

Lane 0 =	DDR2_DQ(7:0)	DDR2_DM(0)	DDR2_DQS(0)
Lane 1 =	DDR2_DQ(15:8)	DDR2_DM(1)	DDR2_DQS(1)
Lane 2 =	DDR2_DQ(23:16)	DDR2_DM(2)	DDR2_DQS(2)
Lane 3 =	DDR2_DQ(31:24)	DDR2_DM(3)	DDR2_DQS(3)

Feedback Clocks

Core-to-DQS Re-sync Clock = DDR2_SYNC_CLK

Routing Rules

1. All signals within a given “Byte Lane Group” should be matched length from the pin on the Stratix II (U13) to the pin on DDR2 Device (U28 or U29). Maximum deviation is +/- 0.050 inches.
2. Keep the distance from the pin on the DDR2 Device (U1 or U2) to the termination resistor pack (to 0.9V_DDR2) to less than 750 mils.

3. Keep the distance from the pin on Stratix II (U13) to the termination resistor pack (to 0.9V_DDR2) to less than 1250 mils.
4. All signals must match lengths between pins (as in (1) above) within +/- 0.250 inches (address, control, data, all byte groups, etc…) Only nets within a byte lane group must be matched tighter as in rule 1. Feedback Clocks are an exception – see rule 10.
5. All signals (other than Address/Command Group) are to maintain a spacing that is based on its parallelism with other nets. This is as follows:
    a. 5 mils for parallel runs < 0.5 inches (~1X spacing relative to plane distance)
    b. 10 mils for parallel runs between 0.5 and 1.0 inches (~2X spacing relative to plane distance)
    c. 15 mils for parallel runs between 1.0 and 6.0 inches (~3X spacing relative to plane distance)
6. All signals are to maintain 20 mil separation from other, non-related nets
7. All signals must have a total length of less than 6 inches.
8. All signals listed in the Address/Command Group should maintain a spacing that is based on its parallelism with other nets but more stringent than in rule 5(a/b/c) above. This is as follows:
    a. 10 mils for parallel runs < 0.5 inches (~1X spacing relative to plane distance)
    b. 15 mils for parallel runs between 0.5 and 1.0 inches (~2X spacing relative to plane distance)
    c. 20 mils for parallel runs between 1.0 and 6.0 inches (~3X spacing relative to plane distance)
9. All signals in the Clock Group must be routed differentially (5 mil trace, 10-15 mil space on centers) and be equal to or up to 100-mils longer than signals in the Address/Command Group.
10. Feedback clock DDR2_SYNC_CLK should be within 100-mils of the average length of the Byte Lane Groups.
11. All signals that are double-loaded (one connection to Stratix II and two connections to DDR2) such as DQ, DQS, DM signals should be routed in a Y-shaped connection with the memory-side termination resistor. The general idea is shown in Figure 4-1

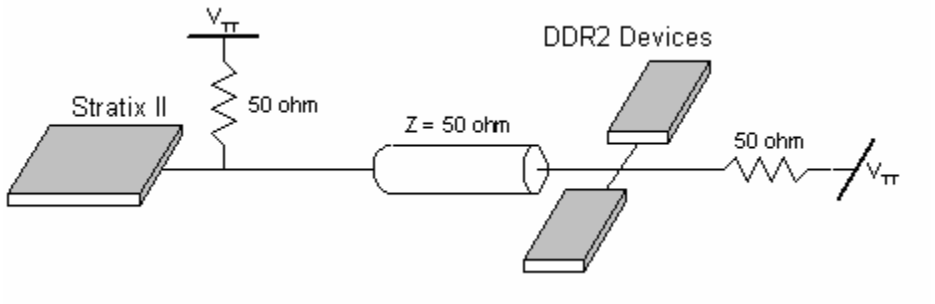


Figure 4-1

12. Within a given Y-shaped connection as described in the previous rule there must be some symmetry and matching within stubs in these traces. These stubs are shown in Figure 4-2 below. In this case the leg L1 should be a majority of the trace. Legs L2 and L3 should be matched within +/- 0.030 inches. The length rule for matching within a group (read group or write group) is NOT the total length of this trace. It is the length of EITHER L1 and L2 or L1 and L3. The connection in the center where all four stubs come together should be routed as shown below (not a 90-degree connection but a 45 degree connection). Leg L4 should be less than 0.750 inches. This should be followed for DDR2 address, command, and control lines.

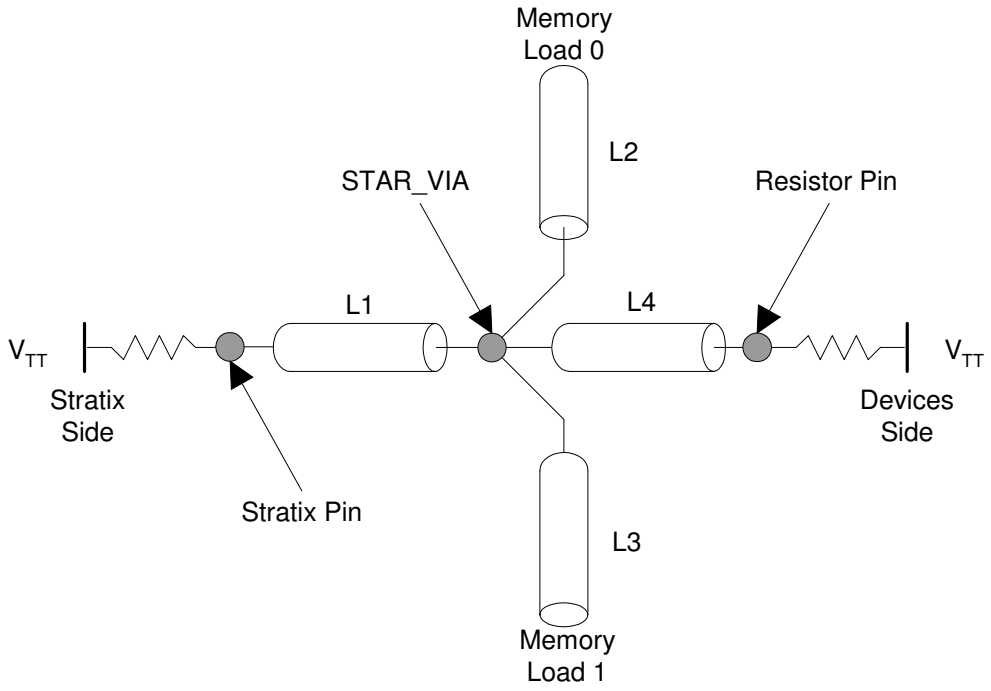


Figure 4-2

4.4.2. QDRII Devices

The following signals run between the QDRII Devices (U30, U36) and the Stratix II FPGA (U13). The trace groups are similar to the DDR2 Devices but the data group signals are double-loaded and here the control signals have a copy for each of the two devices.

Address/Control Group

Address =	QDRII_A(18:0)	
Write Port Select =	QDRII_WPS(1:0)	
Read Port Select =	QDRII_RPS(1:0)	
Byte Write Select =	QDRII_BWS(1:0)	

Write Group

Read Data =	QDRII_Q(17:0)	

Write Group

Write Data =	QDRII_D(17:0)	

Clock Group

Write Clocks =	QDRII_K_P(1:0)	2 rising edge data clocks
	QDRII_K_N(1:0)	2 falling edge data clock
Read Clocks (PLL) =	QDRII_CQ_P(1)	Bottom side device
	QDRII_CQ_N(1)	Bottom side device
Read Clocks (DQS) =	QDRII_CQ_P(0)	Top side device
	QDRII_CQ_N(0)	Top side device

From the above signals a set of groups are made. Each group represents a byte of data and an associated clock and mask control. These will become groups of signals that are length-matched as described below.

QDRII Match Groups

Write Group =	QDRII_D(17:0)	QDRII_K_P(1:0)	QDRII_K_N(1:0)
Read Group =	QDRII_Q(17:0)	QDRII_CQ_P(1:0)	QDRII_CQ_N(1:0)

Feedback Clocks

DQS-to-core Re-sync Clock = QDRII_SYNC_CLK (single-ended)

Routing Rules

1. All signals within a given "QDRII Match Group" should be matched length from the pin on the Stratix II (U13) to the pin on QDRII Device (U30 or U36). Maximum deviation is +/- 0.050 inches. See rule 9 and rule 10 below for clarification on double-loaded signals.
2. Keep the distance from the pin on the QDRII Device (U30 or U36) to the termination resistor pack (to VTT_QDRII) to less than 750 mils.
3. Keep the distance from the pin on Stratix II(U13) to the termination resistor pack (to VTT_QDRII) to less than 1250 mils.
4. **ALL** signals must match lengths between pins (as in (1) above) within +/- 0.200 inches (address, control, data, clocks, etc…) Only nets within a match group must be matched tighter as in rule 1. Feedback clocks are exceptions to this rule – see rule 9.
5. All signals are to maintain a spacing that is based on its parallelism with other nets. This is as follows:
    a. 5 mils for parallel runs < 0.5 inches (~1X spacing relative to plane distance)
    b. 10 mils for parallel runs between 0.5 and 1.0 inches (~2X spacing relative to plane distance)
    c. 15 mils for parallel runs between 1.0 and 6.0 inches (~3X spacing relative to plane distance)
6. All signals are to maintain 20 mil separation from other, non-related nets
7. All signals must have a total length of less than 4 inches.
8. All signals in the Clock Group should be routed single-ended even though they may seem like differential clocks based on their naming conventions. As clock signals they must follow spacing rules as outlined in the CLOCKS section of this document.
9. Feedback clock QDRII_SYNC_CLK should be within 100-mils of the average length of the Byte Lane Groups. All signals in the Feedback Clocks group drive out of the Stratix II (U13) and then back into the Stratix II(U13).
10. All signals that are double-loaded (one connection to Stratix and two connections to QDRII) such as address and control should be routed in a Y-shaped or T-shaped connection with the memory-side termination resistor. The general idea is shown in Figure 4-3.

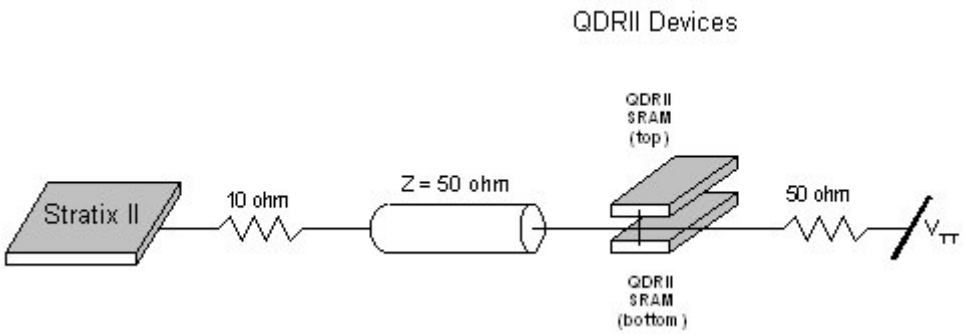


Figure 4-3 (A and control signals)

11. Stratix II output signals that are double-loaded (one connection to Stratix and two connections to QDRII) such as D, K should be routed in a Y-shaped or T-shaped connection with the memory-side termination resistor. The general idea is shown in Figure 4-4.

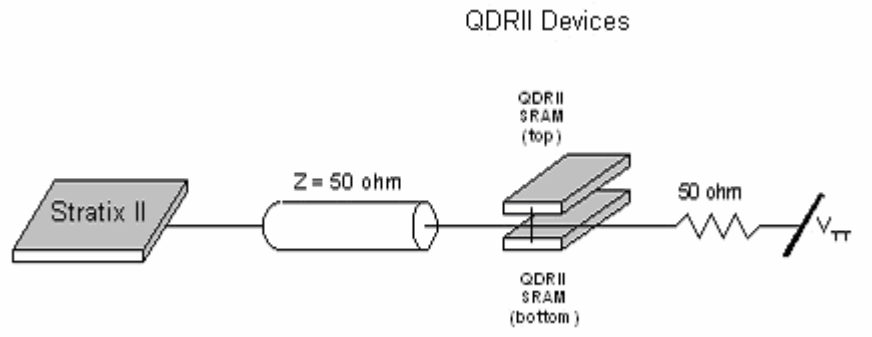


Figure 4-4 (D and K signals)

12. QDRII output signals that are double-loaded (one connection to Stratix and two connections to QDRII) such as Q, CQ should be routed in a Y-shaped or T-shaped connection with the memory-side termination resistor. The general idea is shown in Figure 4-5.

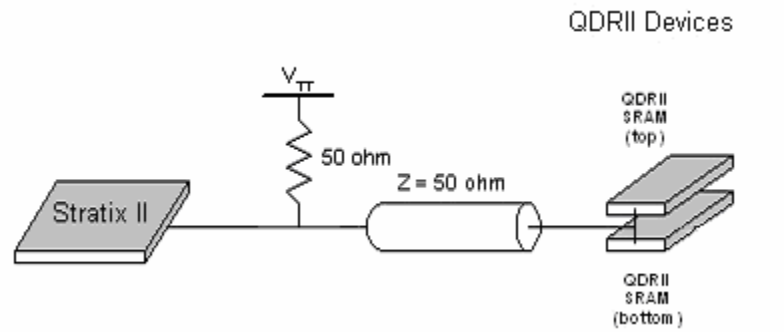


Figure 4-5 (Q and CQ signals)

4.4.3. DDR2 DIMM

The following signals run between the DDR2 DIMM (J15) and the Stratix II FPGA (U13). Signals with similar names such as DIMM_A and DIMM_A_R are the same trace separated by a series resistor. In these cases the overall net length is actually the sum of the two nets.

Address/Command Group

Address =	DIMM_A(15:0)	DIMM_A_R(15:0)
Bank Addr =	DIMM_BA(2:0)	DIMM_BA_R(2:0)
Command =	DIMM_RASn	DIMM_RASn_R
	DIMM_CASn	DIMM_CASn_R
	DIMM_WEn	DIMM_WEn_R

Control Group

Chip Selects =	DIMM_CSn(1:0)	DIMM_CSn_R(1:0)
Clock Enable =	DIMM_CKE(1:0)	DIMM_CKE_R(1:0)
On-Die Term Enable =	DIMM_ODT(1:0)	DIMM_ODT_R(1:0)

Data Group

Data =	DIMM_DQ(63:0)

Data Mask =	DIMM_DM(8:0)		
Data Strobe =	DIMM_DQS(8:0)		
Check Bits =	DIMM_CB(7:0)		

Clock Group

Diff. Clocks =	DIMM_CK_P0	DIMM_CK_N0	(diff pair)
	DIMM_CK_P1	DIMM_CK_N1	(diff pair)
	DIMM_CK_P2	DIMM_CK_N2	(diff pair)

Byte Lane Groups

Lane 0 =	DIMM_DQ(7:0)	DIMM_DM(0)	DIMM_DQS(0)
Lane 1 =	DIMM_DQ(15:8)	DIMM_DM(1)	DIMM_DQS(1)
Lane 2 =	DIMM_DQ(23:16)	DIMM_DM(2)	DIMM_DQS(2)
Lane 3 =	DIMM_DQ(31:24)	DIMM_DM(3)	DIMM_DQS(3)
Lane 4 =	DIMM_DQ(39:32)	DIMM_DM(4)	DIMM_DQS(4)
Lane 5 =	DIMM_DQ(47:40)	DIMM_DM(5)	DIMM_DQS(5)
Lane 6 =	DIMM_DQ(55:48)	DIMM_DM(6)	DIMM_DQS(6)
Lane 7 =	DIMM_DQ(63:56)	DIMM_DM(7)	DIMM_DQS(7)
Lane 8 =	DIMM_CB(7:0)	DIMM_DM(8)	DIMM_DQS(8)

Feedback Clocks

Core-to-DQS Re-sync Clock = DIMM_SYNC_CLK (single-ended)

Routing Rules

1. All signals within a given "Byte Lane Group" should be matched length from the pin on the Stratix II (U13) to the pin on DDR2 DIMM (J15). Maximum deviation is +/- 0.050 inches.
2. Keep the distance from the pin on the DDR2 DIMM (J15) to the termination resistor pack (pull-up to 0.9V_DIMM) to less than 750 mils.
3. Keep the distance from the pin on Stratix II(U35) to the termination resistor pack (pull-up to 0.9V_DIMM or Series Resistor) to less than 1250 mils.
4. All signals must match lengths between pins (as in (1) above) within +/- 0.250 inches (address, control, data, all byte groups, etc…). Only nets within a byte lane group must be matched tighter as in rule 1. Feedback clocks are different – see rule 10.
5. All signals (other than Address/Command Group) are to maintain a spacing that is based on its parallelism with other nets. This is as follows:
    d. 5 mils for parallel runs < 0.5 inches (~1X spacing relative to plane distance)
    e. 10 mils for parallel runs between 0.5 and 1.0 inches (~2X spacing relative to plane distance)
    f. 15 mils for parallel runs between 1.0 and 6.0 inches (~3X spacing relative to plane distance)
6. All signals are to maintain 20 mil separation from other, non-related nets
7. All signals must have a total length of less than 6 inches.
8. All signals listed in the Address/Command Group should maintain a spacing that is based on its parallelism with other nets but more stringent than in rule 5(a/b/c) above. This is as follows:
    g. 10 mils for parallel runs < 0.5 inches (~1X spacing relative to plane distance)
    h. 15 mils for parallel runs between 0.5 and 1.0 inches (~2X spacing relative to plane distance)
    i. 20 mils for parallel runs between 1.0 and 6.0 inches (~3X spacing relative to plane distance)
9. All signals in the Clock Group must be routed differentially (5 mil trace, 10-15 mil space on centers) and be equal to or up to 100-mils longer than signals in the Address/Command Group.
10. Feedback clock DIMM_SYNC_CLK should be within 100-mils of the average length of the Byte Lane Groups. All signals in the Feedback Clocks group drive out of the Stratix II(U13) and then back into the Stratix II(U13).

5. Silkscreen

5.1. Reference Designators

1. All components to have reference designators placed so they are visible after assembly.
2. Where space is not available a reference designator must be placed as close as possible with a visible line pointing to the component being referenced.
3. Pin 1 should be de-marked with a silkscreen dot and a numeric “1” next to the actual pin.

5.2. Company Name and Logos

The Altera Logo is to be placed on the top-side and be at least 1.5” wide.

The Stratix II Logo is to be placed on the top-side and be about 1” wide, and no larger than Altera logo.

5.3. Board Name and Revision

1. The name “**Stratix II Memory Board II**” is to be placed on the top-side and be at least 1.5” wide. If possible it should be placed directly beneath and centered to the Altera Logo. A revision should be labeled near the board name as “**Rev A**”.

5.4. Serial and Part Numbers

A 3/8” x 1 ¼” box shall be drawn for both a serial number and part number sticker and be placed on the bottom-side and labeled as shown below.

S/N

P/N

5.5. Copyright and Country of Origin

1. The board shall display “MADE IN THE USA” on the bottom side.
2. A copyright symbol should be placed next to “ALTERA” on the bottom-side as shown below.

© 2004 ALTERA CORP.

5.6. PCB Part Number

The engineering part number “100-0310122-01” shall be placed in copper etch on the bottom side of board.

5.7. Other Silkscreen

5.7.1. J47 – QDR Impedance Select (sheet 4)

Pin 1-2 → “50 ohm”
Pin 3-4 → “60 ohm”
Pin 5-6 → “Max Drive”

5.7.2. J39 – SMT / Oscilator Select (sheet 10)

Pin 1-2 → “SMT”
Pin 2-3 → “SKT”

5.7.3. J36 – SMA / Oscillator Select (sheet 10)

Pin 1-2 → “OSC”
Pin 2-3 → “SMA”

5.7.4. J27 – PLL Enable (sheet 10)

Pin 1-2 → “EN”
Pin 2-3 → “DIS”

5.7.5. J40 – JTAG Bypass Jumper (sheet 11)

Keep the table on the PCB back-side from the pervious version of the board. Place “see back side” next to jumper.
Pin 3-4 and Pin 1-2 → Stratix II
Pin 1-3 and Pin 2-4 → MAX & Stratix II
Pin 3-5 and Pin 4-6 → EXP & Stratix II

5.7.6. J12, D5, D4 - RS-232 Channel A (sheet 16)

“RS232 CH A” near J12
“TX” near D5
“RX” near D4

5.7.7. J19, D11, D10 - RS-232 Channel A (sheet 16)

“RS232 CH B” near J19
“TX” near D11
“RX” near D10

5.7.8. S1 – Board Setting DIP Switch

“Board Settings” near S1
Pin 1 → “MPGM0”
Pin 2 → “MPGM1”
Pin 3 → “MPGM2”
Pin 4 → “RUnLU”
Pin 5 → “MSEL0”
Pin 6 → “MSEL1”
Pin 7 → “MSEL2”
Pin 8 → “MSEL3”

5.7.9. S4 – User DIP Switch

"USER DIPSWITCH" above S4
"7 6 5 4 3 2 1 0" below S4, with a line or "bathtub" demarking these numbers to the switch.

5.7.10. D19, D20, D21, D22, D23, D24, D25, D26 - USER LEDs

"7 6 5 4 3 2 1 0" below the LEDs respectively with a line or "bathtub" demarking these LED labels the LEDs themselves.

5.7.11. D12, D13, D14, D15, D16, D17 – CONFIG LEDs

D12 → "CONF DONE"
D13 → "FLASH CE"
D14 → "USER DES"
D15 → "LOADING"
D16 → "SAFE DES"
D17 → "ERROR"
If possible place a box around this section.

5.7.12. S3, S2 – RESET Buttons

S3 → "SYS RESET"
S2 → "SAFE"

5.7.13. S5, S6, S7, S8 – USER Buttons

S5 → "PB0"
S6 → "PB1"
S7 → "PB2"
S8 → "PB3"

5.7.14. J46 – QDII I/O Voltage Select

"QDIO" near J46
Pin 1-2 → "1.5V"
Pin 2-3 → "1.8V"

5.7.15. J41 – QDRII I/O Regulator Disable

"QDIO" near J41
Pin 1-2 → "EN"
Pin 2-3 → "DIS"

5.7.16. SW1 – Power Switch

"POWER" near SW1
"ON" near pin 1
"OFF" near pin 6

5.7.17. J10 – 1.2V Regulator Disable

"1.2V" near J10
Pin 1-2 → "EN"
Pin 2-3 → "DIS"

5.7.18. J11 – 1.8V Regulator Disable

"1.8V" near J11
Pin 1-2 → "EN"
Pin 2-3 → "DIS"

5.7.19. J16 – 3.3V Regulator Disable

"3.3V" near J16
Pin 1-2 → "EN"
Pin 2-3 → "DIS"

5.7.20. J34 – DDR2 VTT Regulator Disable

"VTT" near J34
Pin 1-2 → "EN"
Pin 2-3 → "DIS"

5.7.21. J28 – QDRII VTT Regulator Disable

"VTT" near J28
Pin 1-2 → "EN"
Pin 2-3 → "DIS"

5.7.22. J14 – DIMM VTT Regulator Disable

"VTT" near J14
Pin 1-2 → "EN"
Pin 2-3 → "DIS"

5.7.23. J25 – Fan Power Header

"FAN" near J25
Pin 1 → "TACH"
Pin 2 → "12V"
Pin 3 → "GND"

5.7.24. SMA Labels

J52 → "QDRSMA"
J53 → "DDR2SMA"
J46 → "DIMM SMA"
J47 → "DIMM SMA"
J26 → "CLK IN"
J51 → "TRIGGER"
J41 → "PLL6_OUT0_P"
J40 → "PLL6_OUT0_N"
J45 → "PLL6_FB_P"
J44 → "PLL6_FB_N"
J54 → "DLL REF"
J43 → "CLK4_P"
J42 → "CLK4_N"

6. Drawings

6.1. Fabrication Drawing

Place engineering part number "140-0310122-01" in the title block of the fabrication drawing.

Include impedance table.

Include the following fabrication drawing notes:

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALTERA PCB PART NUMBER: P/N 100-0310112-01 REV. A.
2. THIS DRAWING IS VIEWED FROM THE PRIMARY OR TOP SIDE OF PCB.
3. FABRICATION OF THIS PCB SHALL BE IN CONFORMANCE WITH THE FOLLOWING SPECIFICATIONS: IPC-6011 CLASS 2 (GENERIC).
4. FABRICATION OF THIS PCB TO BE ACCEPTABLE TO IPC-A-600 CLASS 2 (LATEST REVISION).
5. ALL DIMENSIONAL LIMITS APPLY AFTER PLATING OR PROCESSING.
6. TOLERANCES OF DATUM HOLE TO:
    a) BOARD EDGE LOCATIONS +/-0.010
    b) DRILLED HOLE LOCATIONS +/-0.003
    c) V-SCORE LOCATIONS +/-0.010 (IF APPLICABLE)
7. BASE MATERIAL: FR4 GLASS EPOXY, MIN. Tg OF 170 DEGREES C.
8. FLAME CLASS: UL 94V-0 & MUST MEET REQUIREMENTS OF UL796.
9. MANUFACTURER MUST BE UL RECOGNIZED TO PRODUCE THIS PRODUCT SUCH THAT IT MEETS 170 DEGREES CELSIUS MAXIMUM OPERATING TEMPERATURE. (MOT).
10. THE FOLLOWING MUST BE MARKED OR ETCHED ON SECONDARY SIDE OF PCB IN AREA SHOWN:
    a) DATE CODE.
    b) UL RECOGNIZED VENDOR ID.
    c) UL TYPE DESIGNATION AND/OR MARKINGS WHICH REFLECT THE SPECIFIED FLAME CLASS AND MAXIMUM OPERATING TEMPERATURE RATINGS.
11. BOW & TWIST SHALL BE DETERMINED BY PHYSICAL MEASUREMENT AND PERCENTAGE CALCULATION IN ACCORDANCE WITH IPC-TM-650. METHOD 2.4.22. BOW & TWIST MAY NOT EXCEED 0.7%.
12. HOLE/SLOT PLATING = 0.001 MIN. AVERAGE / 0.0008 ABSOLUTE MIN. PLATING. HOLE/SLOT DIAMETERS ARE SPECIFIED AFTER PLATING (SEE HOLE SCHEDULE).
13. SMEAR REMOVAL SHALL NOT ETCH BACK GREATER THAN 0.001.
14. INTERNAL ANNULAR RING 0.001 MINIMUM. EXTERNAL ANNULAR RING 0.002 MINIMUM. BOTH ARE MEASURED AT LINE TO PAD ENTRY. NON-FUNCTIONAL INNER LAYER PADS MAY BE REMOVED. SNOWMAN/TEAR DROPPING OF TRACE TO PAD JUNCTION IS PERMITTED PROVIDED MINIMUM METAL-TO-METAL ARTWORK SPACINGS ARE NOT COMPROMISED.
15. FINISHED CONDUCTOR WIDTH NOT TO BE REDUCED MORE THAN 20% OF MINIMUM WIDTH FROM ARTWORK SUPPLIED. FINISHED CONDUCTOR SPACING NOT TO BE REDUCED MORE THAN 20% OF MINIMUM SPACING FROM ARTWORK SUPPLIED.
16. SOLDER MASK IS LIQUID PHOTO IMAGEABLE WITH GLOSSY FINISH AND COLORED GREEN IN ACCORDANCE WITH IPC-SM-840C CLASS T. REGISTRATION TO BE WITHIN +/-0.003 OF ITS RESPECTIVE OUTER CIRCUIT LAYERS. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) TO PROVIDE UP TO 0.003" MAXIMUM CLEARANCE FROM MASK TO PAD PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENTING/PLUGGING" REQUIREMENTS (IF APPLICABLE). NOTE THAT THERE ARE AREAS ON PRIMARY SIDE THAT ARE CLEAR OF SOLDERMASK. SECONDARY SIDE WILL REQUIRE VIAS TO BE EXPOSED.
17. FINISH IS SOLDER MASK OVER BARE COPPER (SMOBC) ON BOTH SIDES WITH 150 MICRO INCHES MINIMUM ELECTROLESS NICKEL (Ni) FOLLOWED BY 3-8 MICRO INCHES IMMERSION GOLD (Au).
18. SILKSCREEN USING WHITE NONCONDUCTIVE INK. NO INK TO APPEAR ON EXPOSED COPPER SUCH AS PLATED THROUGH-HOLE PADS AND SURFACE MOUNT LANDS. INK ON SOLDER MASK COVERED PADS IS PERMISSIBLE. CLIPPING OF SILKSCREEN 0.008 MAX. FROM PADS IS PERMITTED IF REQUIRED.
19. 100% CONTINUITY AND ISOLATION ELECTRICAL TESTING PER CURRENT IPC TEST METHODS REQUIRED FOR EVERY PCB. FINAL PCB TEST DATA MST BE CROSS-REFERENCED TO IPC-D-356 FILE. NEUTRAL FILE OR NETLIST PROVIDED.
20. CONTROLLED IMPEDANCE LINES ARE AS FOLLOWS:
    a) TOLERANCE (ALL LINES) +/-10%.
    b) SINGLE ENDED TRACES TO BE 50 OHMS FOR 5 MILS TRACE ON ALL LAYERS.
    c) EDGE COUPLED DIFFERENTIAL TRACES TO BE 100 OHMS FOR:
        5 MIL TRACE 17 MIL CENTER TO CENTER SPACING ON EXTERNAL LAYERS.
        5 MIL TRACE 10 MIL CENTER TO CENTER SPACING ON INTERNAL LAYERS.
21. VENDOR TO PROVIDE ONE TEST COUPON AND ONE CROSS SECTION PER LOT WITH SHIPMENT.
22. VENDOR TO PROVIDE 2 SOLDER SAMPLES WITH FIRST SHIPMENT.
23. DETAILS NOT SPECIFIED ARE AT MANUFACTURER'S OPTION. HOWEVER FINAL APPROVAL MUST BE OBTAINED.
24. THESE HOSES MAY BE PLATED SHUT OR SOLDER FILLED.
25. PLUG VIA HOLES FROM PRIMARY SIDE WITH SR-1000 OR EQUIVALENT MATERIAL. CLEAR UV MASK IS ACCEPTABLE. PLUG HEIGHT NOT TO EXCEED 0.003 OVER FINISHED PLATING HEIGHT.
26. COPPER THIEVING SHALL BE APPLIED WHEREVER REQUIRED BUT MUST HAVE A SPACING OF 100 MILS FROM ANY OTHER COPPER FEATURE ON THE BOARD.

27. REMOVE ALL UNCONNECTED VIA PADS IN INNER LAYERS.
28. DELIVERY. PROVIDE 6 BOARDS TO ALTERA AND 2 BOARDS TO FLEXTRONICS FOR SMT AND THERMAL TESTING.

6.2. Assembly Drawing

Place engineering part number “130-0310122-01” in the title block of the assembly drawing.

Include the following assembly drawing notes:

NOTES: UNLESS OTHERWISE SPECIFIED

1. ASSEMBLE BOARD PER IPC-A-610(LATEST REVISION) STANDARD.
2. HANDLE MOISTURE SENSITIVE DEVICES (MSD) PER MANUFACTURER’S CALL OUT ON MSD LABEL. IF MSD LABEL IS MISSING OR NOT LEGIBLE THEN ALL PLASTIC PACKAGED COMPONENTS ARE TO BE CONSIDERED MSD LEVEL 6 AND USE EIA/JEP 113-A FOR HANDLING.
3. REWORK MUST BE APPROVED BY CUSTOMER BEFORE BEING ACCEPTABLE. USE IPC-R-700 (LATEST REVISION) FOR ALL PCA REWORK APPROVED.
4. SQUARE PIN PAD DENOTES PIN 1 OF ICs/CONNECTORS. POSITIVE END FOR CAPACITORS OR CATHODE END FOR DIODES.
5. INSTALL BAR CODE LABEL APPROX. WHERE SHOWN. INCLUDING S/N.